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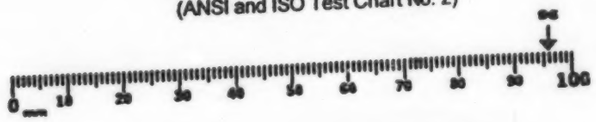

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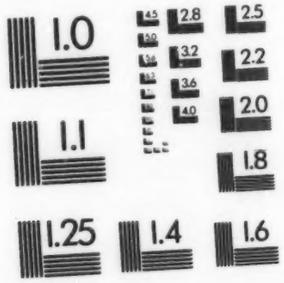

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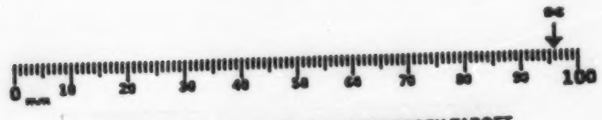

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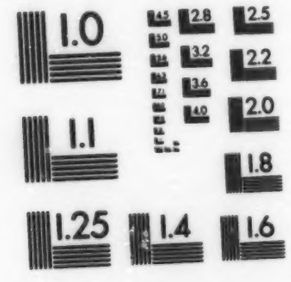

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DEFENCE R&D DÉFENSE

Design and Measurement of a 44.5 GHz PHEMT Power Amplifier

Scott R. McLelland and Malcolm G. Stubbs
Terrestrial Wireless Systems
Research Integrated Electronic

Gilbert A. Morin
Military Satellite Communications Group
Space Systems and Technology Section

CRC Communications Research Centre
Centre de recherches sur les communications

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TECHNICAL REPORT
DREO TR 2000-112
CRC Report No. 2000-001
November 2000

Abstract

The work described in this report represents the design phase of a gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier using pseudomorphic high electron mobility transistors (PHEMTs). The main purpose was to investigate the possible performance of a power amplifier at 44 GHz for future application in a phased array antenna system. The design of a two stage amplifier, covering the frequency range 43.5 - 45.5 GHz, is described along with measured results. The final layout of the complete chip is also presented.

Resumé

Ce projet décris les étapes de conceptions d'un amplificateur de puissance utilisant la technologie de fabrication de circuit monolithic sur l'Arsenure de Gallium (GaAs MMIC) avec des transistors à effet de champ à hétérostructure pseudomorphic (PHEMT). Le but principale était de déterminer les performances réalisable d'un amplificateur de puissance à 44 GHz qui pourrait ensuite être utilisé comme composante d'une antenne réseau. La conception d'un amplificateur à deux étages, couvre la bande de fréquences de 43.5 à 45.5 GHz, est décris avec les résultats. Le plan final du circuit est aussi présenté.

Executive Summary

The design procedure for a 44.5 GHz gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier is presented. The MMIC is intended for the transmit portion of a communications Transmit/Receive module currently being developed. This report outlines the initial determination of the appropriate transistor size and its bias conditions in order to meet the amplifier specifications. Non-linear design techniques, used to predict the performance of the amplifier at its maximum power level of operation, are also introduced. Input and output matching networks are developed and the predicted amplifier performance, including associated bias networks, is presented. The final amplifier layout is shown and the amplifier performance predictions are confirmed through the use of an electromagnetic simulation design tool. Finally the amplifier is shown to be cascadable allowing sufficient gain to be achieved for a driver stage application.

The amplifier was fabricated by Northrop Grumman using a 0.25 μm PHEMT process. There was, however, a delay of over one year due to severe process problems. A first wafer was fabricated that did not pass process control monitor (PCM) specifications. Measurements of the amplifiers varied across the wafer but the overall shape of the amplifier measurements was as expected indicating the design was valid. Specifically, the gains were lower than expected and the center frequency of the amplifier was shifted lower. A second set of wafers that did meet PCM specifications was also delivered. Measurements of amplifiers on these wafers also varied across each wafer and were, in general, slightly worse than the amplifiers that did not pass PCM specifications. After consideration of the results and given the process equipment problems, the worse than expected performance and variability of the amplifiers are likely due to process variations beyond our control.

Clearly, further design iterations are needed and this is not uncommon in MMIC design. Often multiple design iterations are needed in order to account for unexpected process variations and simulation inaccuracies. Indeed, the higher the design frequency, the higher the uncertainty is.

McLelland, S. R., Stubbs, M. G., and Morin, G. A., 2000. *Design and Measurement of a 44.5 GHz PHEMT Power Amplifier*, DREO TR 2000-112, CRC RP 2000-001, Defence Research Establishment Ottawa.

Sommaire

Ce rapport présente une procédure de conception d'un amplificateur de puissance à 44.5 GHz utilisant la technologie de fabrication de circuit monolithique sur l'arséniure de gallium (GaAs MMIC). Ce circuit MMIC sera utilisé dans le partie de transmission d'un module émission/réception pour un système de communications. Ce rapport détaille la détermination initiale des dimensions des transistors ainsi que les conditions de polarisation pour atteindre les spécifications de l'amplificateur. Des techniques de conception non-linéaire sont utilisées pour prédire les performances de l'amplificateur opérant à sa puissance maximale. Des réseaux d'adaptation en entrée et en sortie, incluant les réseaux de polarisations, ont été developpé. Le schéma de l'amplificateur final est présenté, ainsi que les prédictions initiales de ses performances. Un simulateur électromagnétique est utilisé pour confirmer les performances prédites de l'amplificateur. Finalement, il est démontré que l'amplificateur peut être utilisé en cascade et qu'il a suffisamment de gain pour être utilisé dans l'étage de commande.

L'amplificateur a été fabriqué par Northrop Grumman en utilisant le procédé PHEMT (transistor à effet de champ à hétérostructure pseudomorphic) de 0.2 μm. Malheureusement, la compagnie a rencontré de sérieux problèmes avec ce procédé et la fabrication a été retardé d'un an. La première plaquette fabriquée n'a pas passé les tests de contrôle de procédé (PCM). Des mesures micro-ondes des amplificateurs ont quand même été réalisées et l'ensemble des résultats valide la conception malgré certains problèmes: le gain est plus faible que prévu et la fréquence de résonance est plus basse. Une deuxième quantité de plaquettes fut fabriquée et rencontra les spécifications PCM. Les résultats des mesures micro-ondes sont très comparables mais un peu moins bonnes que les mesures précédentes. Après avoir analysé les résultats en détail, il a été déterminé que les variations dans le procédé de fabrication sont responsables des variations observées dans les mesures.

Evidemment, d'autres itérations seraient nécessaires pour améliorer la performance de l'amplificateur, ce qui est très courant dans la conception MMIC. Ceci est encore plus important aux ondes millimétriques où les modèles de transistors fournis par le manufacturier sont en général moins précis qu'à plus basses fréquences.

McLelland, S. R., Stubbs, M. G., and Morin, G. A., 2000. *Design and Measurement of a 44.5 GHz PHEMT Power Amplifier*, DREO TR 2000-112, CRC RP 2000-001, Centre de recherches pour la défense Ottawa, DREO.

Table of Contents

Abstract iii

Resumé iii

Executive Summary v

Sommaire vi

Table of Contents vii

List of Figures and Tables ix

I. Specifications 1

II. Design 1

A. Amplifier Topology 1
DC Bias 1
Small Signal Analysis 1
Large Signal Analysis 4

B. Amplifier Matching Networks 7
Device Input/Output Models 7
Broadband Matching Using Models 8
Narrowband Matching using Models 11

C. Bias networks, chokes and dc blocking capacitors 16

D. Amplifier Small Signal Performance 17

E. Amplifier Stability 18

F. Amplifier Schematics 19

G. Amplifier Large Signal Performance 24

H. Electromagnetic Simulations 25

I. Amplifier Layout 28

J. Amplifier With Interconnects 28
Dual Amplifier Chain Performance 33

III. Fabricated Circuits 34

IV. Measurements 35

A. Wafer 1 35

B. Wafers 3, 4 & 5 35

V. Conclusions 36

Appendix A: Performance of Individual Chips on Wafer 1 Versus Frequency 37

Appendix B: Performance of Multiple Chips (wfr0 and jig0) on Wafer 1 Versus Frequency 42

Appendix C: Performance of Multiple Chips on Wafer 3 Versus Frequency 46

Appendix D: Performance of Multiple Chips on Wafer 4 Versus Frequency 48

Appendix E: Performance of Multiple Chips on Wafer 5 Versus Frequency 50

Appendix F: PCM Data for Wafers 3, 4 and 5 52

List of Figures and Tables

Figure 1: Simulated I-V curves for a 300 μm Northrop Grumman PHEMT 2
Figure 2: Maximum available gain of various device sizes 2
Figure 3: Small signal S-parameters of various device sizes 3
Figure 4: Small signal stability of various device sizes 3
Figure 5: Load pull of single 300 μm device (12 dBm input power) 5
Figure 6: Comparison of output power for optimum power load and conjugately matched load for a 300 μm device 5
Figure 7: Load pull of a single 300 μm device with 3V drain bias 6
Figure 8: Input model for a 300 μm PHEMT from 41.5 GHz to 47.5 GHz 7
Figure 9: Output model of a single 300 μm PHEMT from 41.5 GHz to 47.5 GHz 8
Figure 10: Ideal broadband input matching network 8
Figure 11: Ideal broadband input match simulations 9
Figure 12: Ideal broadband output matching network 9
Figure 13: Ideal broadband output match simulations 10
Figure 14: Ideal broadband interstage matching network 10
Figure 15: Ideal broadband interstage match simulations 11
Figure 16: Smith Chart of input match using ideal elements 12
Figure 17: Smith Chart of output match using ideal elements 13
Figure 18: Input matching network with microstrip elements after optimization 13
Figure 19: Input matching performance with microstrip elements and input model termination 14
Figure 20: Output matching network with microstrip elements after optimization 14
Figure 21: Output matching performance with microstrip elements and output model termination 15
Figure 22: Interstage matching network in microstrip (dc blocking capacitor assumed transparent) 16
Figure 23: Interstage matching performance with microstrip elements and with the input and output models as terminations 16
Figure 24: Input and output match of the two stage amplifier 17
Figure 25: Small signal gain of the two stage amplifier 18
Figure 26: Amplifier Stability 19
Figure 27: Final two stage amplifier schematic 20
Figure 28: Final input matching network schematic 21
Figure 29: Final interstage matching network schematic 22
Figure 30: Final output matching network schematic 23

Figure 31: Output power as a function of input power over the desired bandwidth.....24
Figure 32: EM simulated amplifier performance after optimization 26
Figure 33: EM simulated amplifier performance after optimization 26
Figure 34: Amplifier large signal performance after EM optimization 27
Figure 35: Amplifier stability from EM analysis.....28
Figure 36: Final two stage amplifier layout 29
Figure 37: Small signal performance of the amplifier with interconnects (after EM optimization).....30
Figure 38: Small signal performance of the amplifier with interconnects (after EM optimization).....30
Figure 39: Large signal performance of the amplifier with interconnects (after EM optimization).....31
Figure 40: Stability of the amplifier with interconnects (after EM optimization).....31
Figure 41: Final layout of the amplifier with interconnects.....32
Figure 42: Small signal return loss performance of two amplifier chain with interconnects 33
Figure 43: Small signal gain performance of two amplifier chain with interconnects 33
Figure 44: Photograph of power amplifier intended for wafer probing.....34
Figure 45: Photograph of power amplifier intended for measurement in a jig.....34
Figure 46: SSPA S-parameters vs frequency [Jig = R3C5, V_D = 2.0 volts, V_G = -0.5 volt, I_{DS} = 221 mA] 37
Figure 47: SSPA S-parameters vs frequency [Jig = R2C2, V_D = 2.0 volts, V_G = -0.5 volt, I_{DS} = 150 mA] 38
Figure 48: SSPA S-parameters vs frequency [Jig : R5C2. V_D = 1.2 volt, V_G = -0.5 volt, I_{DS} = 131 mA] 39
Figure 49: SSPA S-parameters vs frequency [Jig = R6C7, V_D = 1.4 volts, V_G = -0.6 volt, I_{DS} = 70 mA] 40
Figure 50: SSPA S-parameters vs frequency [Jig = R3C2, V_D = 2.5 volts, V_G = -0.6 volt, I_{DS} = 90 mA] 41
Figure 51: SSPA gain for Wafer 1 - wfr0. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom).....42
Figure 52: SSPA input and output return losses for Wafer 1 - wfr0.....43
Figure 53: SSPA gain for Wafer 1 - jig0. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom).....44
Figure 54: SSPA input and output return losses for Wafer 1 - jig0.....45
Figure 55: SSPA gain for Wafer 3. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom).....46
Figure 56: SSPA input and output return losses for Wafer 3.....47
Figure 57: SSPA gain for Wafer 4. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom).....48

Figure 58: SSPA input and output return losses for Wafer 4.....49
Figure 59: SSPA gain for Wafer 5. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom).....50
Figure 60: SSPA input and output return losses for Wafer 5.....51
Figure 61: PHEMT parameters from manufacturer's documentation 52
Figure 62: PCM data from manufacturer's documentation 53

Table 1: Large signal performance of the two stage amplifier as a function of frequency.....24
Table 2: Large signal performance of the two stage amplifier as a function of frequency after EM optimization 27

I. Specifications

This project was an investigation to determine potential GaAs MMIC amplifier performance around 44 GHz using the Northrop Grumman foundry process. A detailed amplifier specification was not available and target specifications were used to guide the investigation as follows:

Frequency range	43.5 – 45.5 GHz
Power output	100 mW
Gain	> 10 dB
Return loss	> 10 dB on both ports
Size	3 x 2 mm maximum

II. Design

The design process is outlined in the following sections.

A. Amplifier Topology

The amplifier was to be operated in a conventional common source configuration. The device operating point was first chosen and then the performance of various device sizes were compared using small and large signal analyses. The results of this comparison were used to select the device size and number of stages required.

DC Bias

Class A quiescent operation was chosen for linearity and simplicity. The Northrop Grumman Design Manual (hereafter 'the design manual') suggested a typical Class A operating point of 50% I_{DSS}, V_{GS} = -0.5 V and V_{DS} = 5 V and hence this was chosen as the dc operating point. Simulated I-V curves for a 300 µm device are shown in Figure 1.

Small Signal Analysis

Small signal analysis was used to compare device sizes on the basis of gain, input/output impedance and stability. Since small signal S-parameters and maximum available gain (MAG) define the best achievable parameters they were used to compare device sizes. The MAG, S-parameters and stability of various devices is given in Figures 2, 3 and 4 respectively.

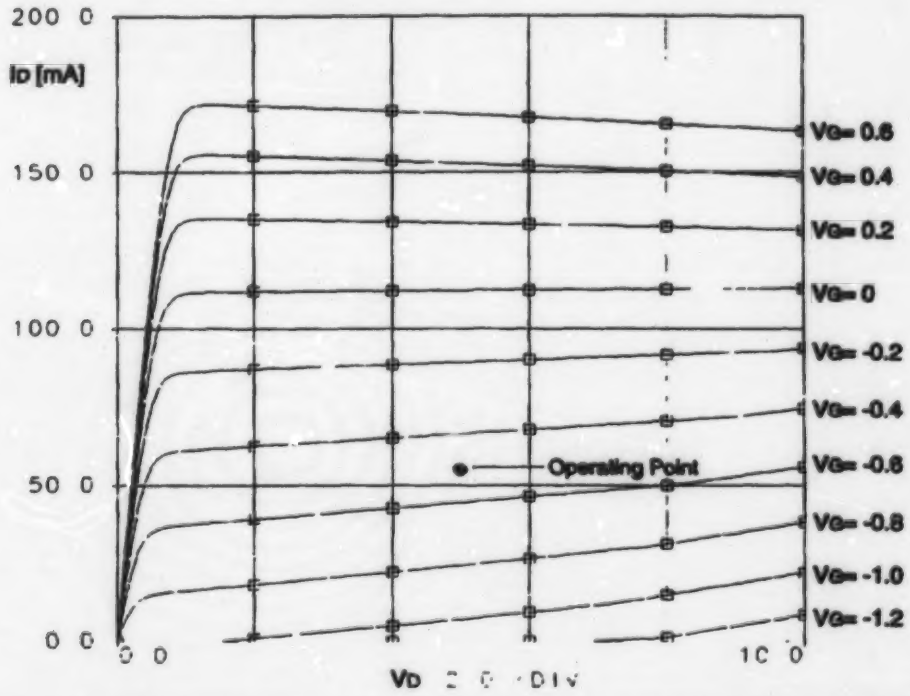

Figure 1: Simulated I-V curves for a 300 μm Northrop Grumman PHEMT

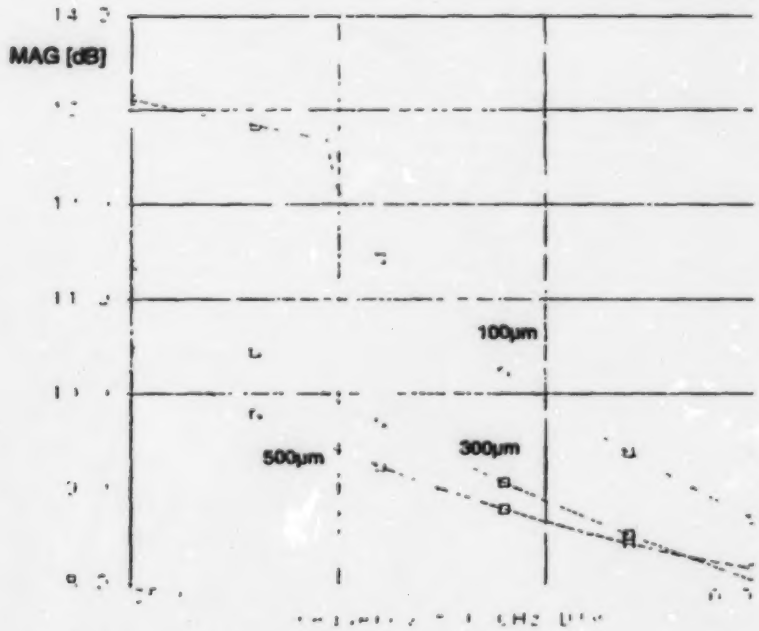

Figure 2: Maximum available gain of various device sizes

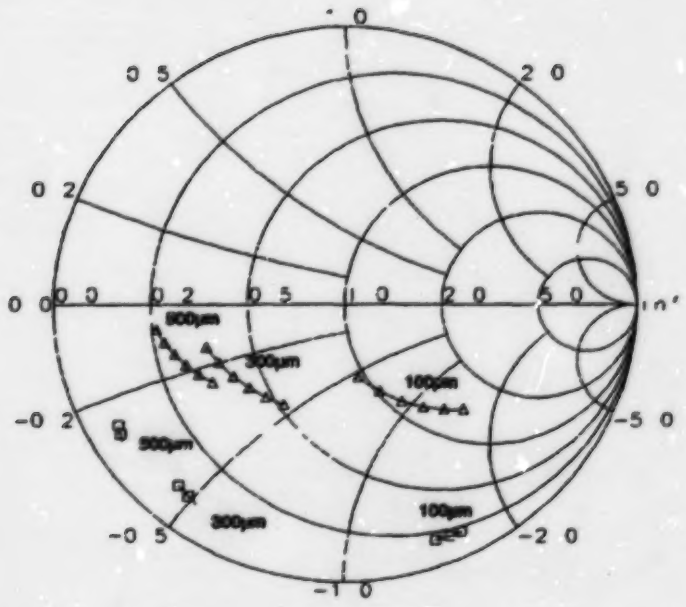

Figure 3: Small signal S-parameters of various device sizes

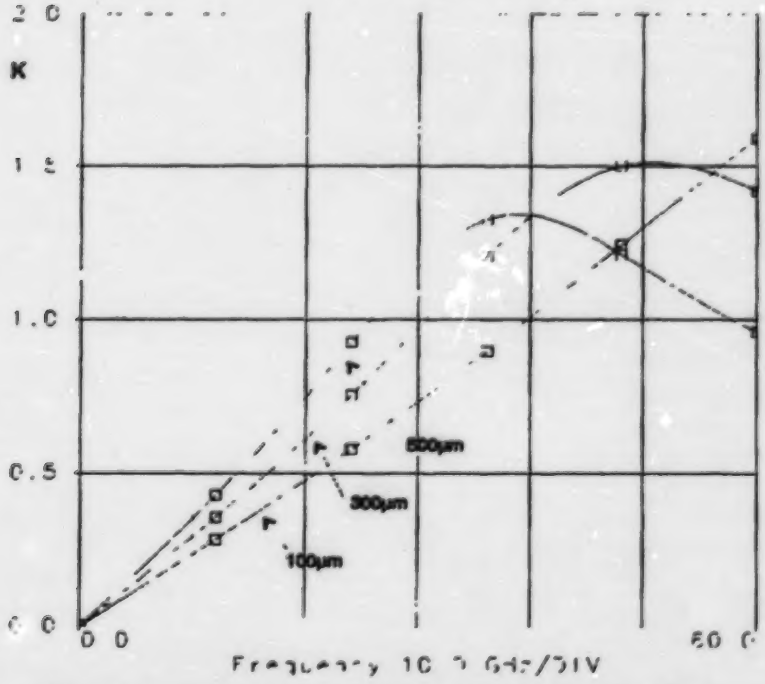

Figure 4: Small signal stability of various device sizes

A preliminary device size of 300 μm was chosen. The design manual provided an approximation of 0.5 W per mm of device gatewidth. It follows that the 300 μm size should give approximately 21.8 dBm of output power and hence meeting the design specification of 20 dBm with some margin. Further, Figure 2 shows that the 300 μm device could provide approximately 9 dB gain and Figure 3 shows that the input and output impedances are well behaved, varying relatively slowly with frequency. Finally, according to Figure 4, the 300 μm device shows instability below approximately 30 GHz (since K<1). However, preliminary analysis indicated that this should be correctable by adding stabilizing resistors behind the chokes since the instability was not in the band of interest.

Large Signal Analysis

The device was then evaluated for large signal performance since the design manual only approximated the output power. A load pull analysis was used to find the maximum output power and the associated optimum power load. The design manual provided an approximate optimum power load at 10 GHz that was scaled to a centre frequency of 44.5 GHz. The device was terminated by this approximate optimum load for power and the input was conjugately matched. The output power, as a function of input power, was simulated using Harmonic Balance techniques, from which the 1 dB compression point was found to be 12 dBm. Using this 1 dB compression point as the approximate input power to the device a load pull analysis was performed and the results are shown in Figure 5.

The load pull analysis confirmed that the 300 μm device should meet the performance requirement with an output power of 20.2 dBm given an optimum normalized load of 0.3+j0.2 Ω. The output power of the device was also considered for the case of the output conjugately matched with a normalized load of 0.18+0.29 Ω. The results are shown in Figure 6, and it is clear that the optimum load provided more output power. However, the small signal gain is only slightly less than the conjugately matched case. This was expected since the optimum load for power is very close to the conjugately matched load.

Given these results the amplifier was matched for optimum power. The amplifier could also be used as a driver since the small signal gain is not significantly smaller than for the conjugately matched load.

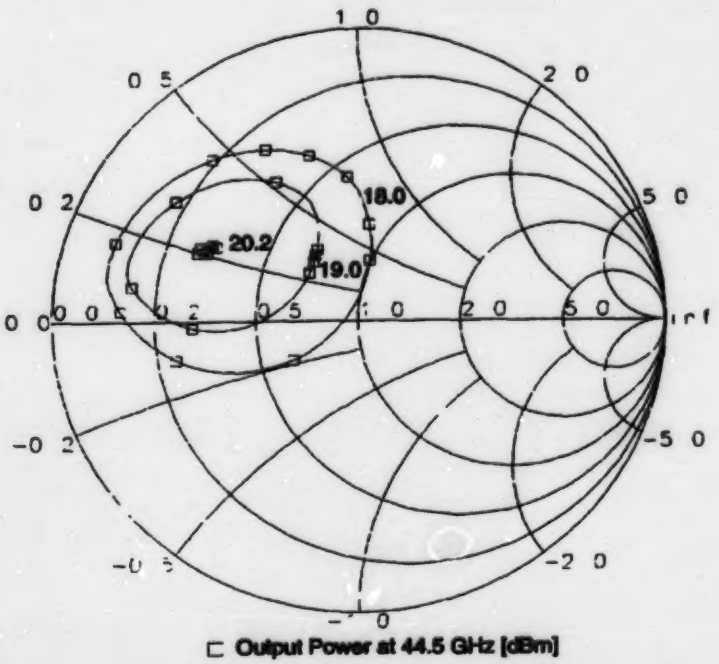

Figure 5: Load pull of single 300 μm device (12 dBm input power)

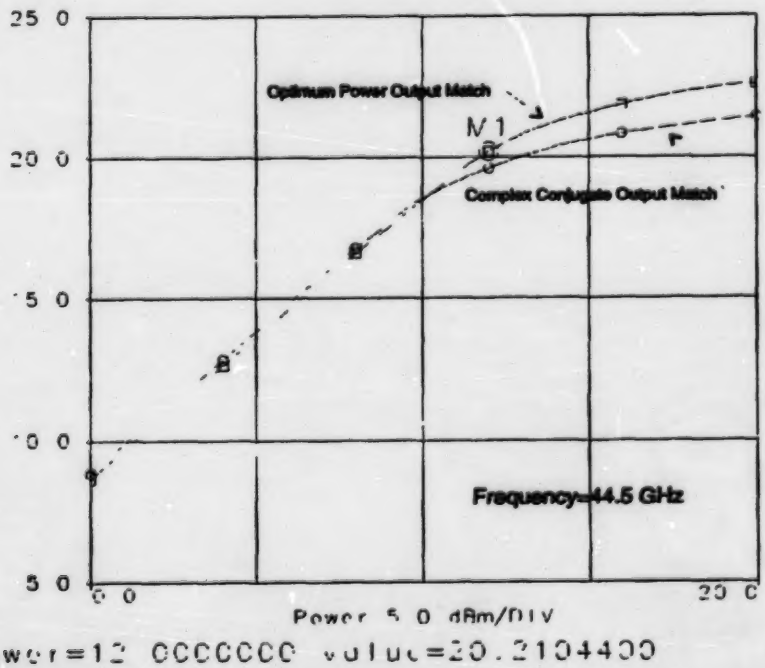

Figure 6: Comparison of output power for optimum power load and conjugately matched load for a 300 μm device

All of the aforementioned analysis was performed at the Class A bias point of 5V on the drain. It was required to investigate if 3V on the drain could achieve the same performance at an increased level of efficiency. Therefore the entire large signal analysis was performed with 3V on the drain. Note that in this case the design manual approximate optimum load was scaled according to frequency and bias. The resulting load pull is shown in Figure 7.

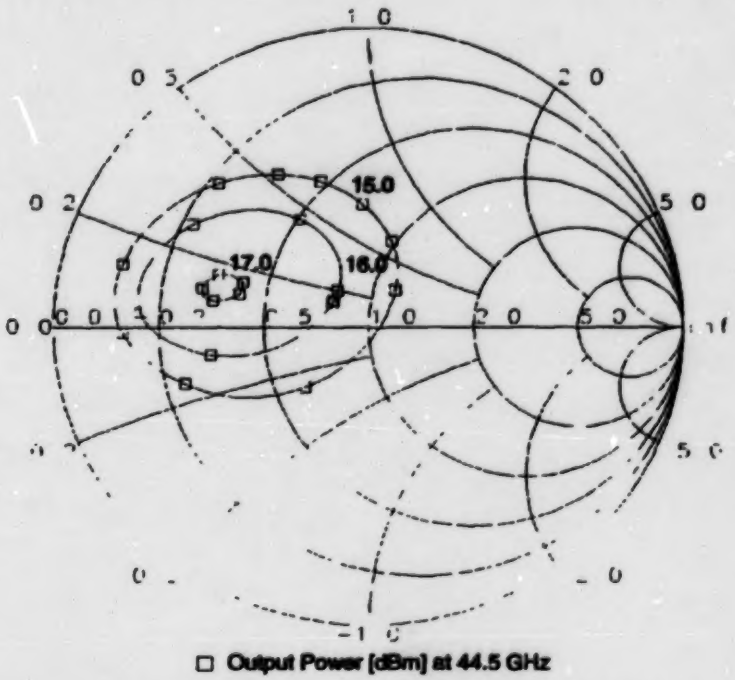

Figure 7: Load pull of a single 300 µm device with 3V drain bias

From Figure 7 the maximum output was 17 dBm and was not sufficient to meet the requirements, hence a drain bias of 5V was selected. Clearly, in order to increase the efficiency another topology such as Class B or C must be used. However, Class A was chosen for simplicity.

In summary, a 300 µm device was selected achieving a gain of up to 9 dB and 20 dBm output power. With the gain known, two stages were selected such that the 20 dBm output power was achieved at a reasonable input power level. A Class A topology was used to reduce the complexity of the overall circuit thereby increasing the likelihood that the measured results will correlate with simulations.

B. Amplifier Matching Networks

After the selection of amplifier topology, the input, output and interstage matching networks were developed. First, the input and output impedances of the device were modeled. Using these models the matching networks were investigated using broadband Q-matching techniques. It will be shown, however, that the broadband techniques did not provide acceptable performance, hence narrowband techniques were used in the final amplifier layout.

Device Input/Output Models

With the input power set at the 1 dB compression point a load pull analysis was performed on a single 300 μm device to find the optimum load for power from 41.5 GHz to 47.5 GHz. This data was then used as a file of reflection coefficients to terminate the output of the device while the input impedance was fitted to an R-C series circuit model. Figure 8 shows the resulting input model for the PHEMT used (all schematics have units of Ω for resistors, nH for inductors, and pF for capacitors). The negative inductance does not result from the modeling itself, it is instead a factor inserted afterwards to account for the overestimation of connecting line inductance in the simulations. The value of the negative inductance was provided by Northrop Grumman and is based on measurements.

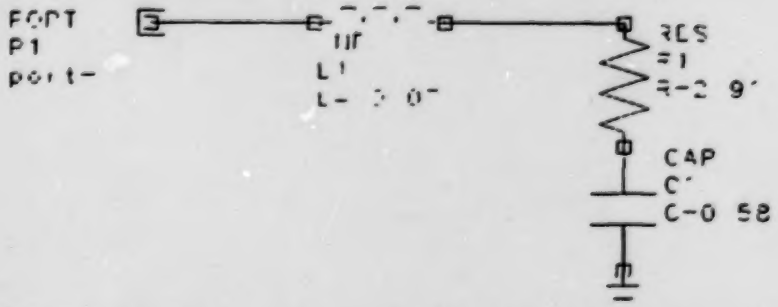

Figure 8: Input model for a 300 μm PHEMT from 41.5 GHz to 47.5 GHz

The output circuit model topology is based on the approximate model provided in the design manual. The model values were optimized to agree to the conjugate of the optimum load reflection coefficient file. The output model is shown in Figure 9.

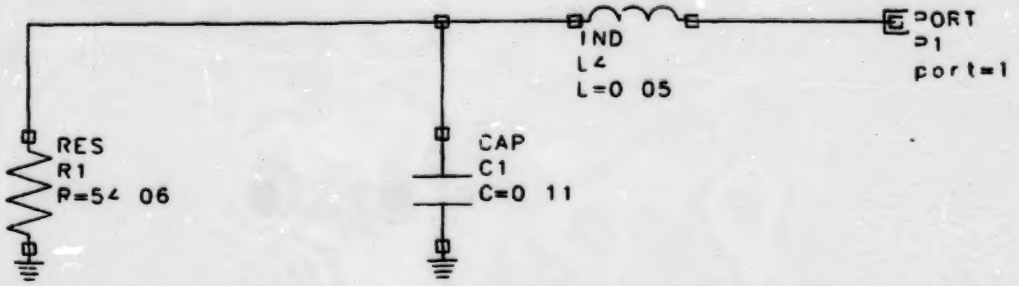

Figure 9: Output model of a single 300 μm PHEMT from 41.5 GHz to 47.5 GHz

Since the optimum load was close to the conjugate match, the outputs of both stages were matched for optimum power to reduce the complexity of the circuit.

Broadband Matching Using Models

Broadband Q-matching was first used in an attempt to design the input, output and interstage matching networks using the device input and output models as terminations. This technique synthesizes a Butterworth response and the resulting ideal input matching network is shown in Figure 10, with its associated performance in Figure 11. The ideal output matching network schematic is given in Figure 12, with its performance in Figure 13. Figure 14 provides the ideal interstage matching network, while Figure 15 shows the ideal interstage match performance.

Figure 10: Ideal broadband input matching network

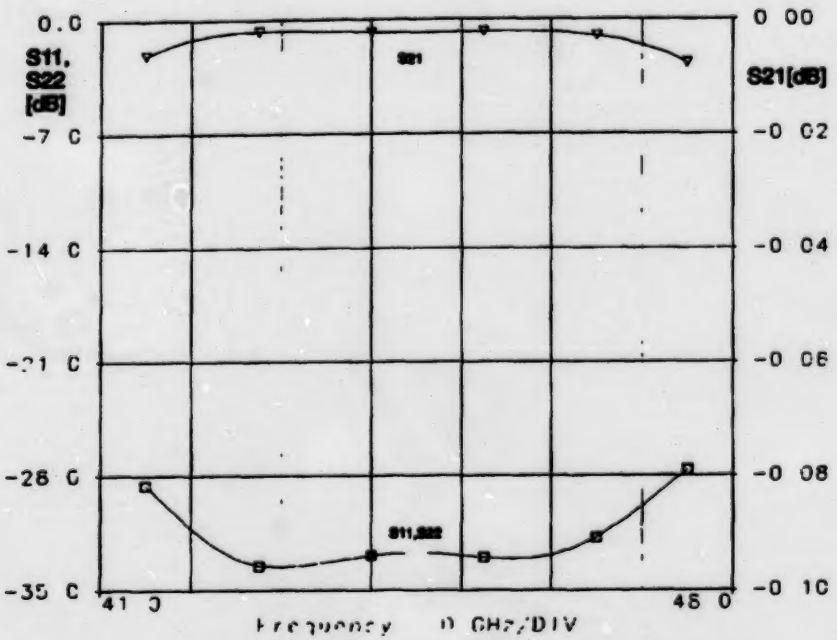

Figure 11: Ideal broadband input match simulations

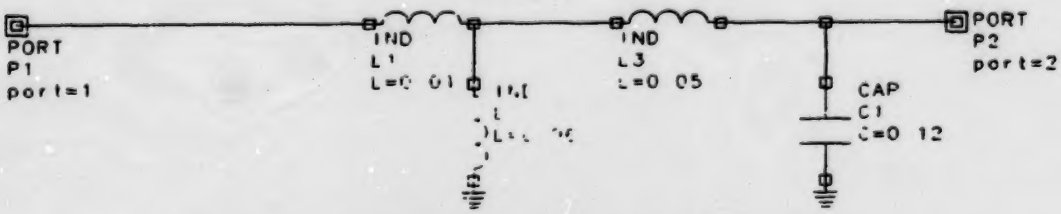

Figure 12: Ideal broadband output matching network

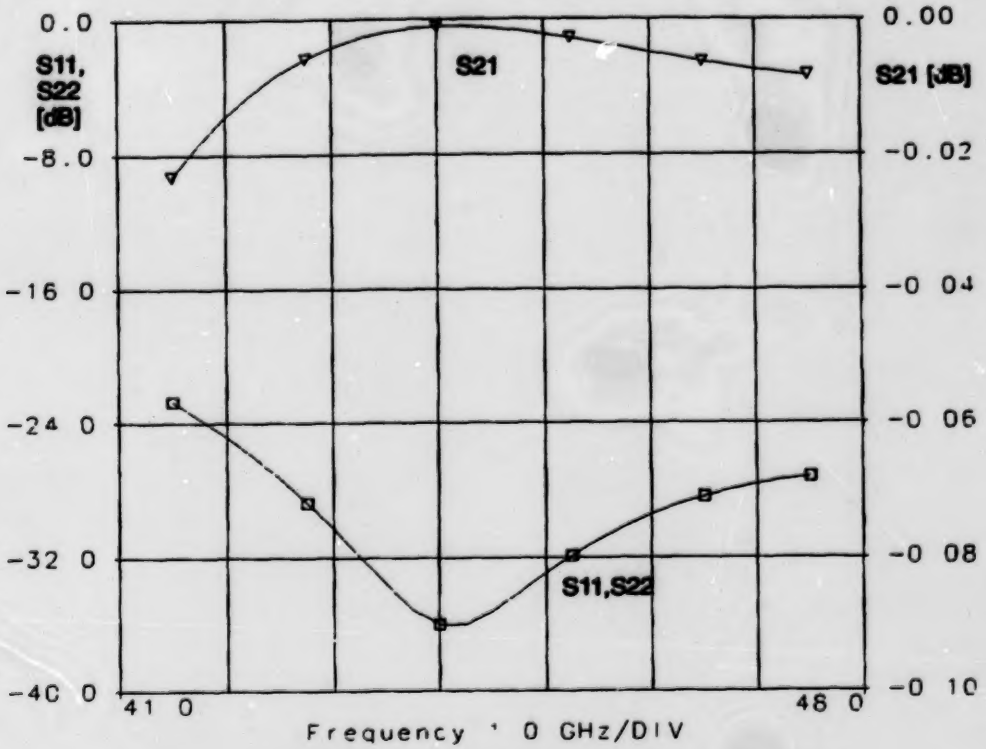

Figure 13: Ideal broadband output match simulations

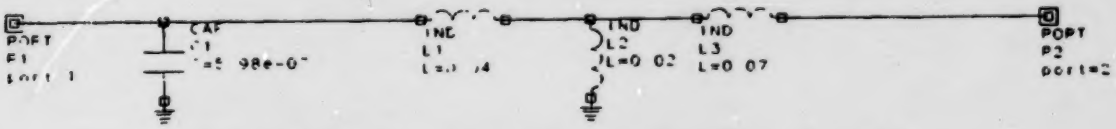

Figure 14: Ideal broadband interstage matching network

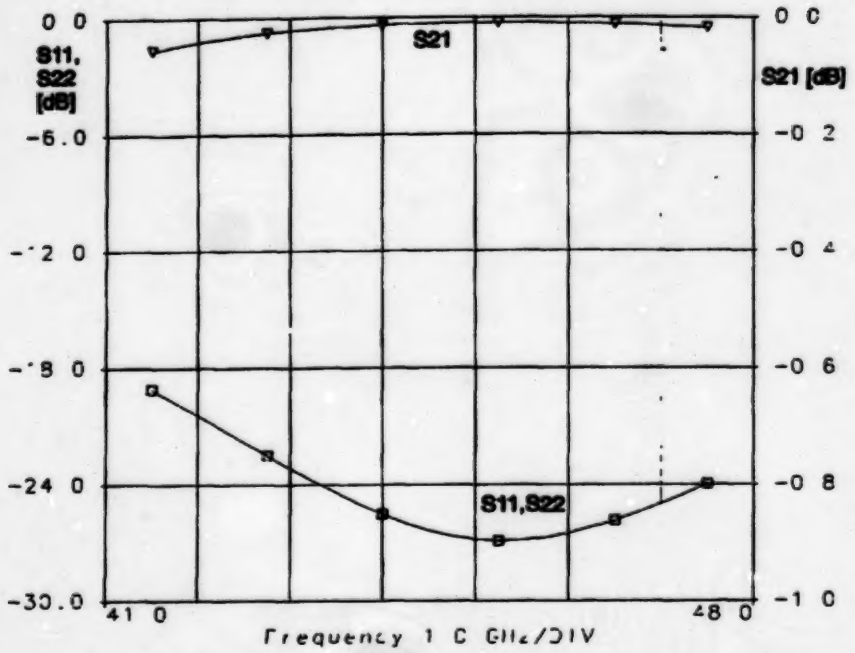

Figure 15: Ideal broadband interstage match simulations

These broadband networks could not be realized with microstrip elements. The required length of transmission line to enter and leave the device structure was too long and hence gave more inductance than could be tolerated by the broadband networks. E-syn™ (a commercial circuit synthesis software package) was used to no avail in an attempt to find other possible broadband topologies. A series capacitor was used to attempt to tune out the additional inductance, however the distributed effect of the capacitor added more inductance, resulting in no improvement. Additionally, a series capacitor was not desirable given the 10 % tolerance of the capacitance and the fact that an exact value was required to resonate with the extra inductance. Coupled lines were also investigated but the distributed inductance nullified the capacitive resonance effect. Therefore, the broadband techniques were abandoned in favour of narrowband techniques.

Narrowband Matching using Models

The Smith Chart was used to design narrowband matching networks by starting at the input or output model of the device and moving to the 50 Ω reference impedance. For a bandpass response giving maximum bandwidth it is desired to alternate between low-pass elements and high-pass elements. Bandwidth is also maximized by staying within the Q-circle of the termination with the larger Q. Unfortunately, the high-pass/low-pass element approach conflicts with the Q-circle condition if realizable transmission line element values are used, e.g. the minimum lengths required to connect to the device itself. This conflict confirmed why the broadband approach failed. It was decided to use only low-

pass elements as they give a more realizable topology while staying within the necessary Q-circle to extend the bandwidth of the match.

Therefore, using the input model as a starting point ideal low-pass transmission line elements were used to move across the Smith Chart to form the match. The resulting input match is shown in Figure 16; note that the input model Q circle of 2.13 is not exceeded. The same procedure was used, with the output model as a starting point, to develop the output match, and the resulting Smith Chart is given in Figure 17. Again the output model Q of 1.6 was not exceeded, and low-pass elements were used.

The electrical lengths of the ideal transmission lines were then used to determine the physical lengths of microstrip transmission lines. Crosses and tees were also added, as were step discontinuities. The microstrip lines were all selected to be 50 Ω, except close to the input of the device where a narrower 25 μm line was required because of the source via holes. Figure 18 shows the final input matching circuit with microstrip elements after optimization, and Figure 19 gives the simulated performance with the input model as a termination. Note that the line between the two stubs was shortened and then removed during the optimization phase.

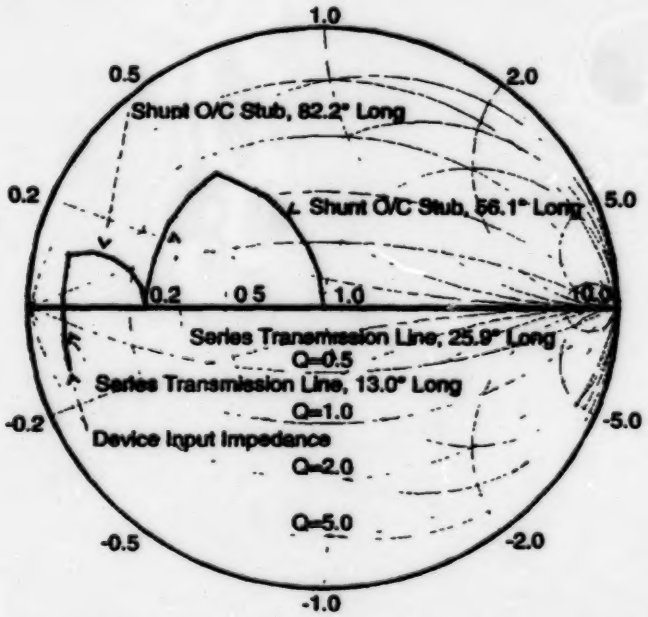

Figure 16: Smith Chart of input match using ideal elements

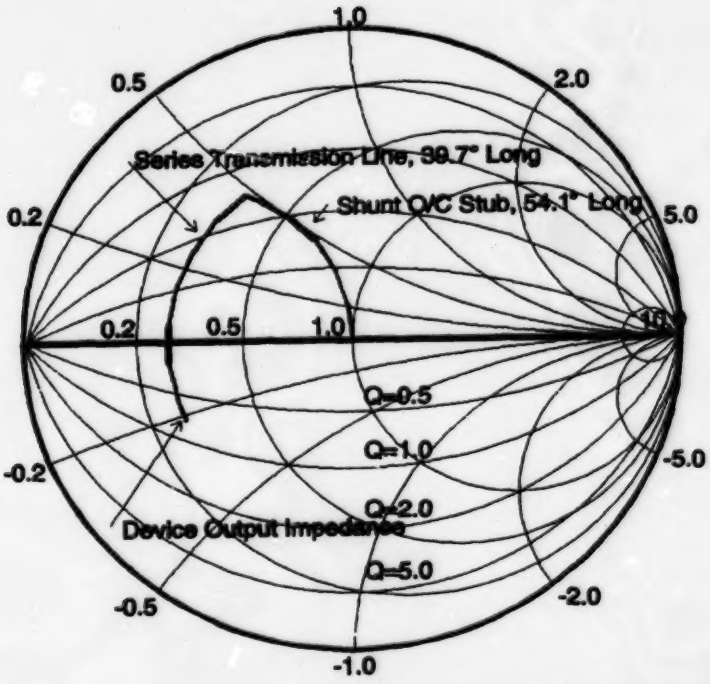

Figure 17: Smith Chart of output match using ideal elements

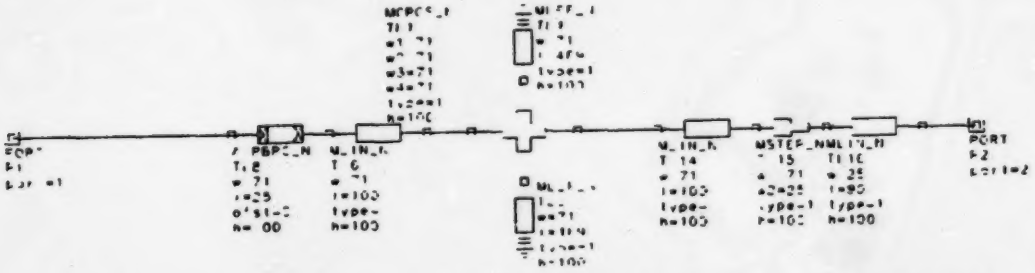

Figure 18: Input matching network with microstrip elements after optimization

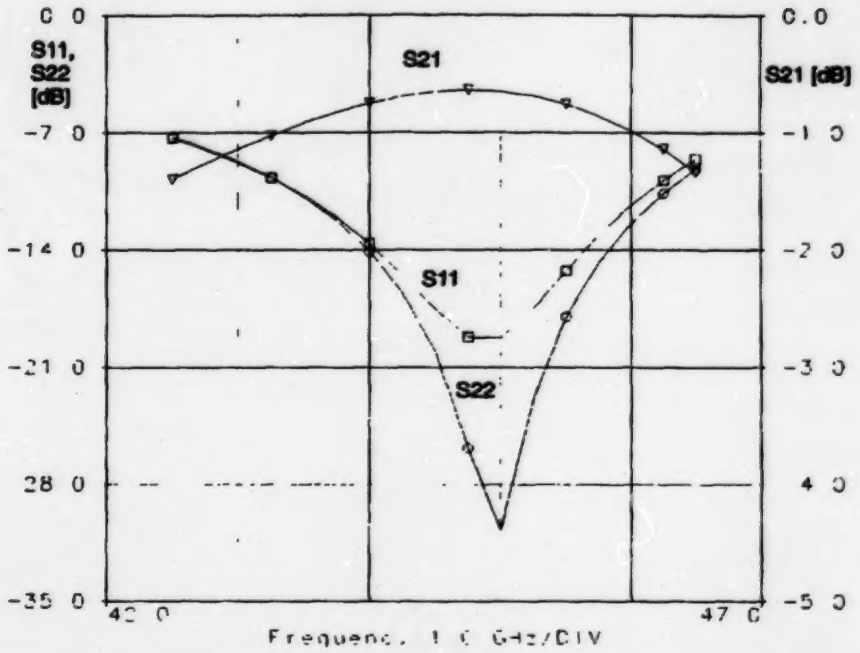

Figure 19: Input matching performance with microstrip elements and input model termination

The final output matching circuit after optimization is provided in Figure 20. The simulated performance of the output matching circuit with the output model as a termination is given in Figure 21.

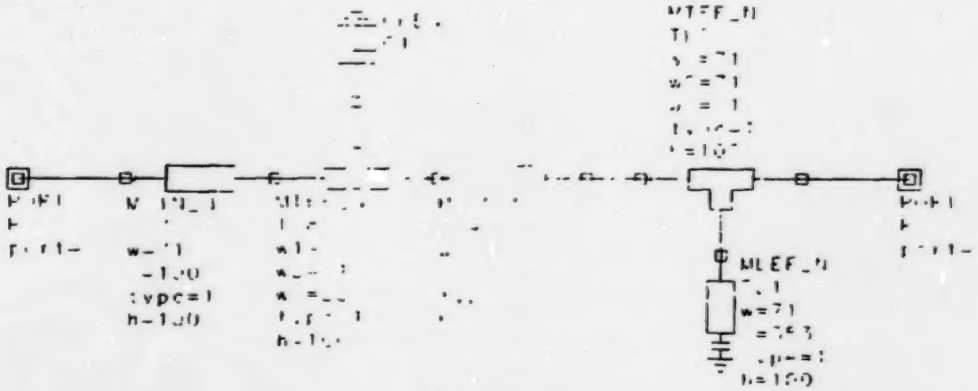

Figure 20: Output matching network with microstrip elements after optimization

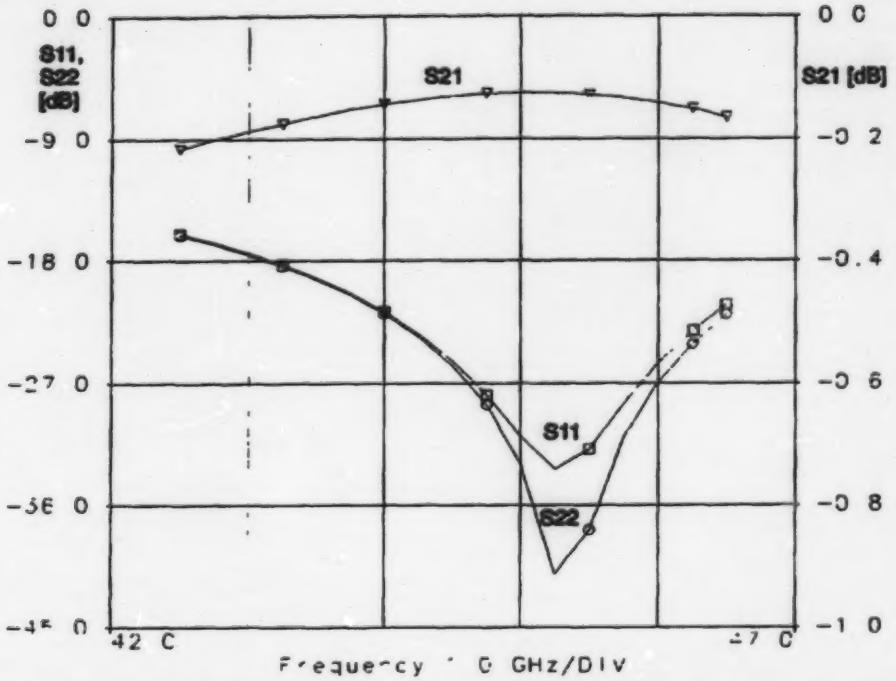

Figure 21: Output matching performance with microstrip elements and output model termination

The interstage matching network was also addressed using the Smith Chart approach, however the resulting network was not realizable. The transmission line lengths were not long enough to provide adequate spacing between the devices. Additionally, the distributed effect from a dc blocking capacitor would force the transmission lines lengths to be further modified. It was decided to use the existing input and output matching networks and match the interstage to an interim value of 50 Ω. This significantly reduces the effect of the dc blocking capacitor, as the distributed effects are minimal if 50 Ω transmission line is used for the capacitor plates within a 50 Ω system at that point. A 71 μm x 71 μm capacitor exactly fits within the width of a 50 Ω transmission (C = 1.84 pF) and the 10% capacitance variation will not significantly affect the impedance or, by extension, the interstage match. The trade-off to this approach is the extra space required. However, the performance improvement justified the extra space.

The interstage matching network, as realized in microstrip, is shown in Figure 22 without the dc blocking capacitor. The simulated performance with the input and output models as terminations is given in Figure 23.

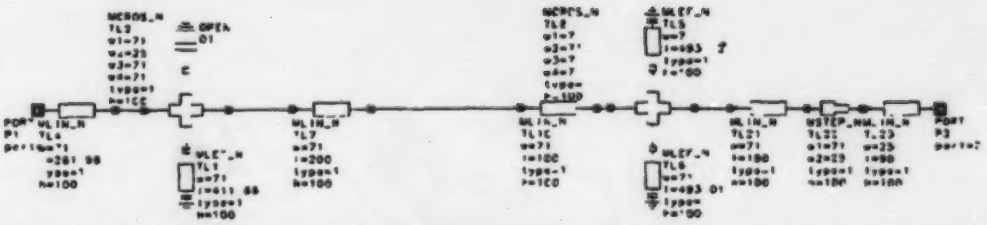

Figure 22: Interstage matching network in microstrip (dc blocking capacitor assumed transparent)

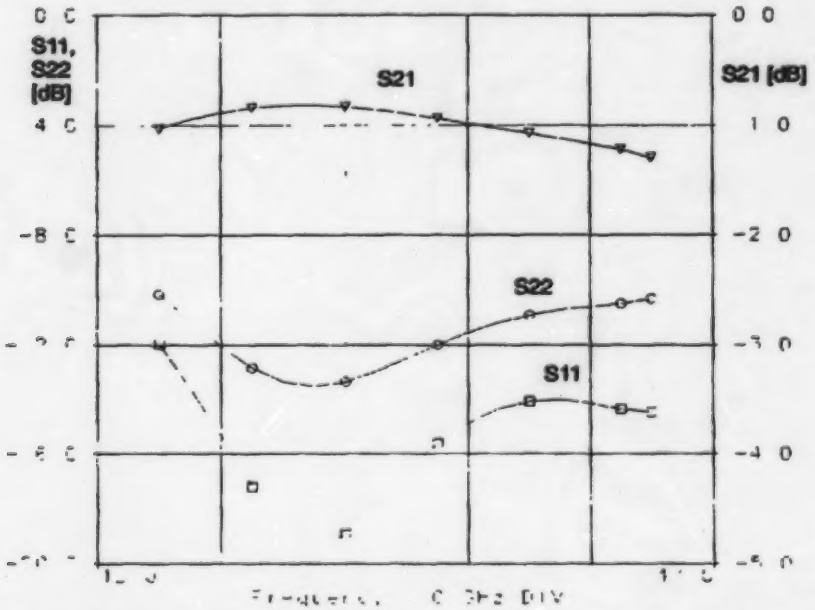

Figure 23: Interstage matching performance with microstrip elements and with the input and output models as terminations

C. Bias networks, chokes and dc blocking capacitors

Quarter wavelength microstrip transmission lines were used as the bias chokes. Large capacitors provided an RF short circuit, while blocking the dc from entering the via hole. The chokes were not bent to increase the accuracy of the simulations.

DC blocking capacitors were added at the input and the output. These capacitors were not included in the input or output matching networks to minimize the affect on overall performance.

The interstage dc blocking capacitor was also placed to minimize its affect on the match by placing it in a region close to 50 Ω where the frequency dependence of the distributed effects is lowered.

The blocking capacitors were used where possible to bring in the dc bias. This avoids using more tee junctions than absolutely necessary.

D. Amplifier Small Signal Performance

The resulting matching networks, blocking capacitors, chokes and bias circuitry were then used in conjunction with the actual non-linear device models to simulate performance. The input, output and interstage matching networks were optimized for gain compensation, input and output match. The final simulated performance of the input and output match for the two stage amplifier is given in Figure 24. The final small signal gain of the two stage amplifier is shown in Figure 25.

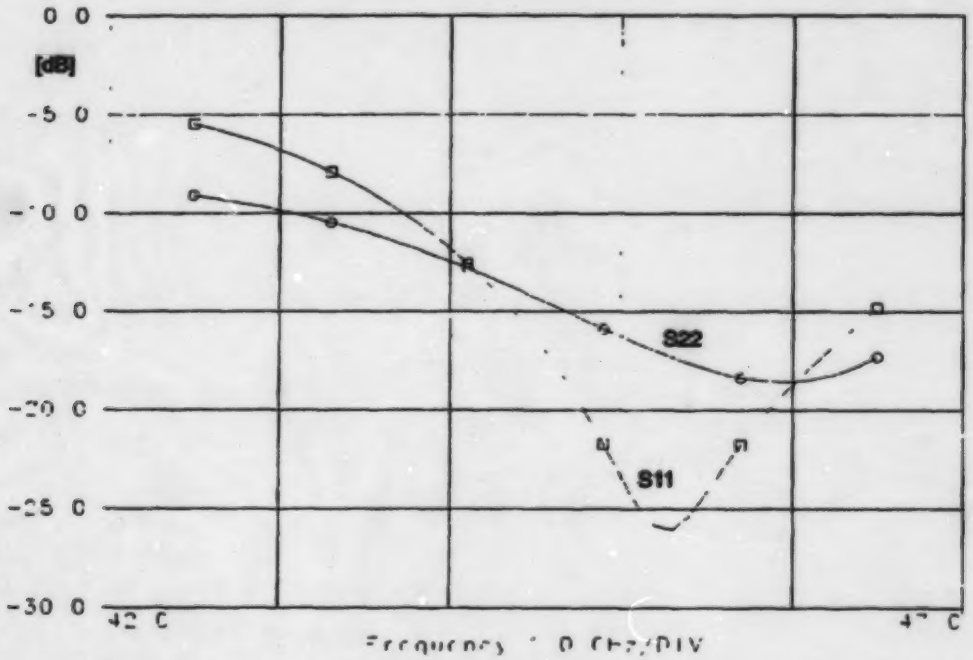

Figure 24: Input and output match of the two stage amplifier

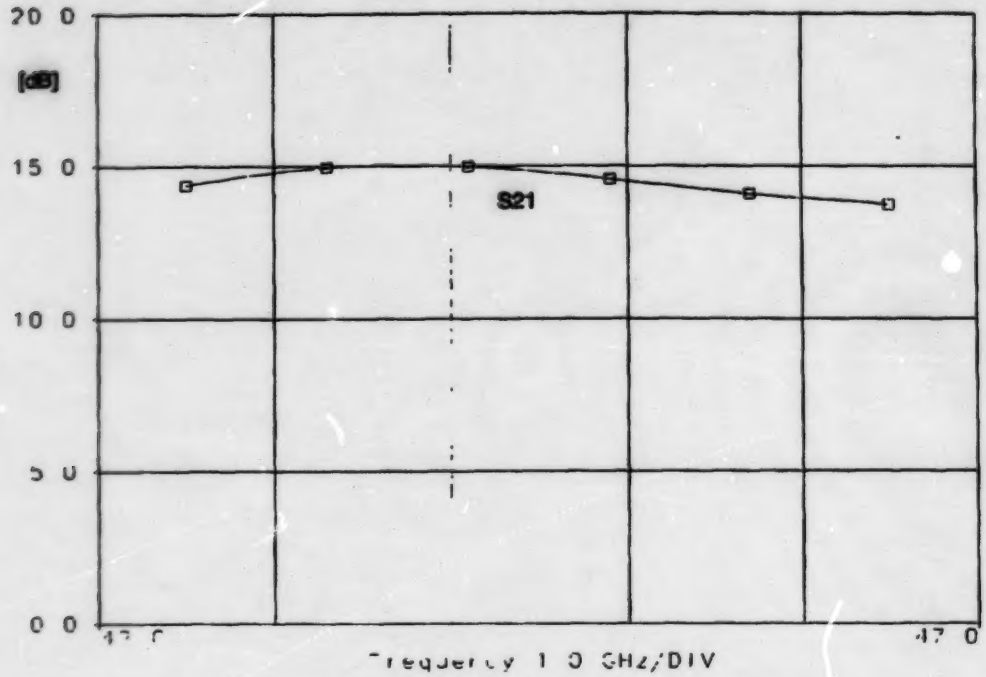

Figure 25: Small signal gain of the two stage amplifier

E. Amplifier Stability

The two stage amplifier was found to be stable within the desired bandwidth of 43.5 GHz to 45.5 GHz, but unstable from 7 GHz to 22 GHz. The out-of-band instability was addressed by adding resistors behind the drain chokes of the two devices. This had the effect of loading the transistors out-of-band thereby reducing the gain and increasing stability. The resistors were added before the RF shorting capacitor since the drain current is quite large and a resistor in the dc path would have reduced the dc bias voltage. The degradation in the RF short due to the presence of this resistor was tolerable. Additionally, the RF shorting capacitors were reduced in size to exactly resonate with the via hole inductance. This provided a narrowerband short in the band of interest and hence further loaded the devices out of band of interest. It should be noted that the value of the capacitor could change with the manufacturing tolerances. However, the increase in stability was worth the trade-off. Furthermore, the via hole capacitor resonance is not very sharp so capacitance variations should be tolerable. The stability of the final two stage amplifier is shown in Figure 26.

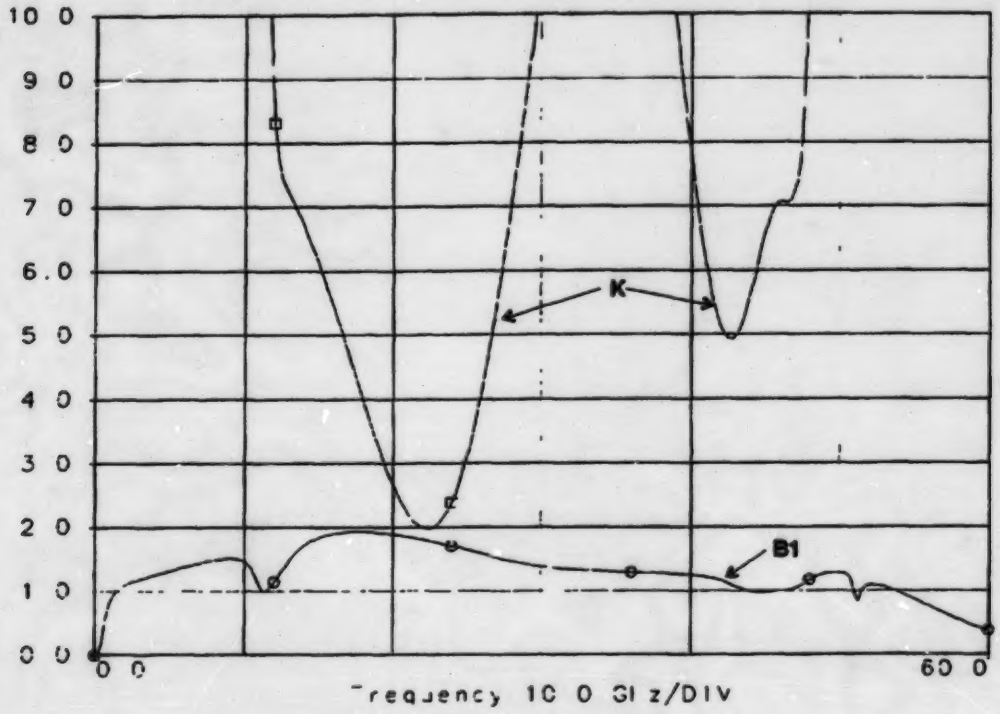

Figure 26: Amplifier Stability

F. Amplifier Schematics

The final simulator schematic of the two stage amplifier is shown in Figure 27. The final input, interstage and output matching network schematics with bias, chokes, stabilizing resistors and blocking capacitors, are shown in Figures 28, 29 and 30 respectively.

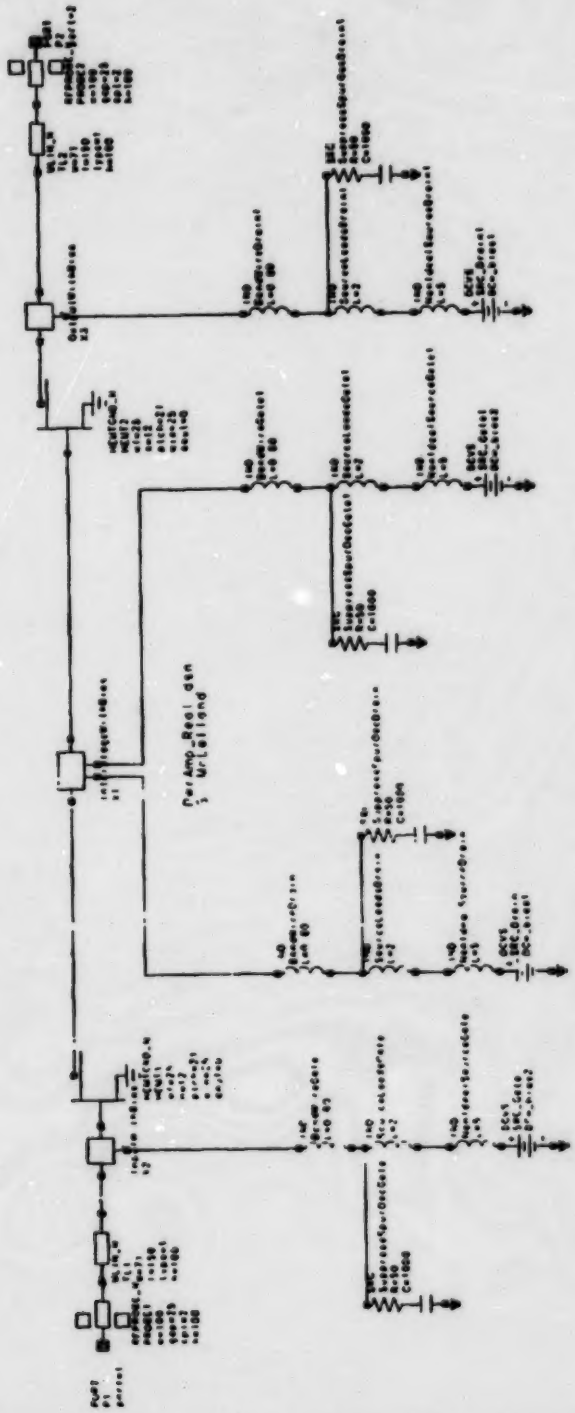

Figure 27: Final two stage amplifier schematic

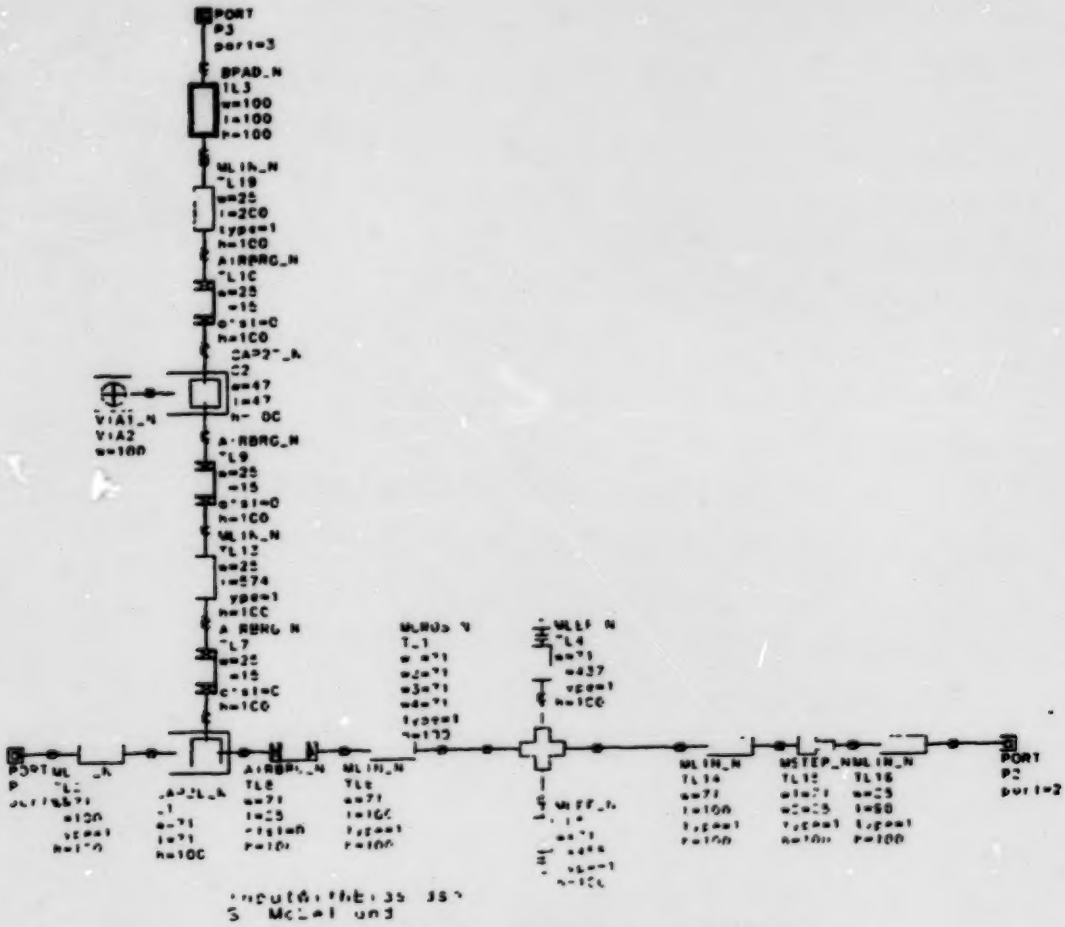

Figure 28: Final input matching network schematic

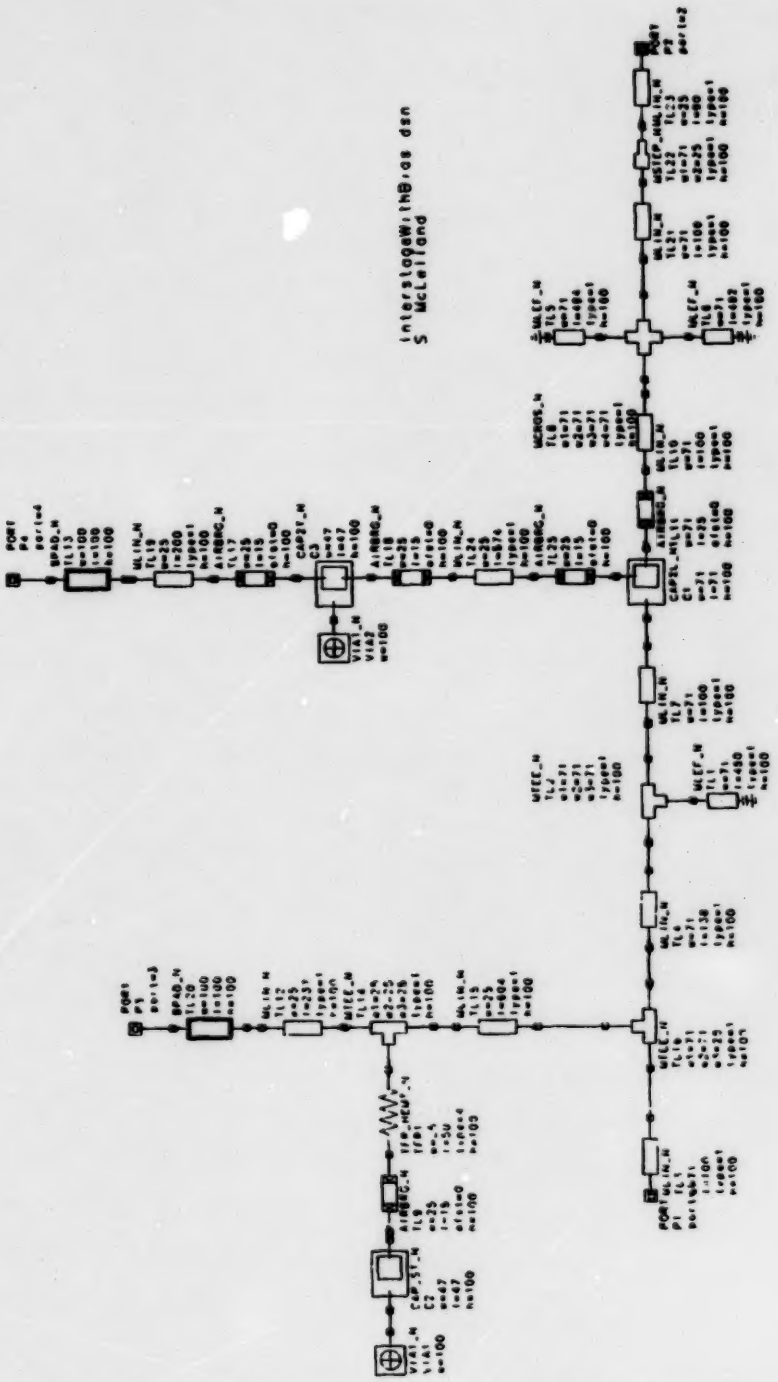

Figure 29: Final interstage matching network schematic

Figure 30: Final output matching network schematic

G. Amplifier Large Signal Performance

The amplifier was simulated using harmonic balance to analyze its large signal behavior. The resulting P_{out} versus P_{in} curves are shown in Figure 31. For 20 dBm output power, the input power and gain as a function of frequency is provided in Table 1.

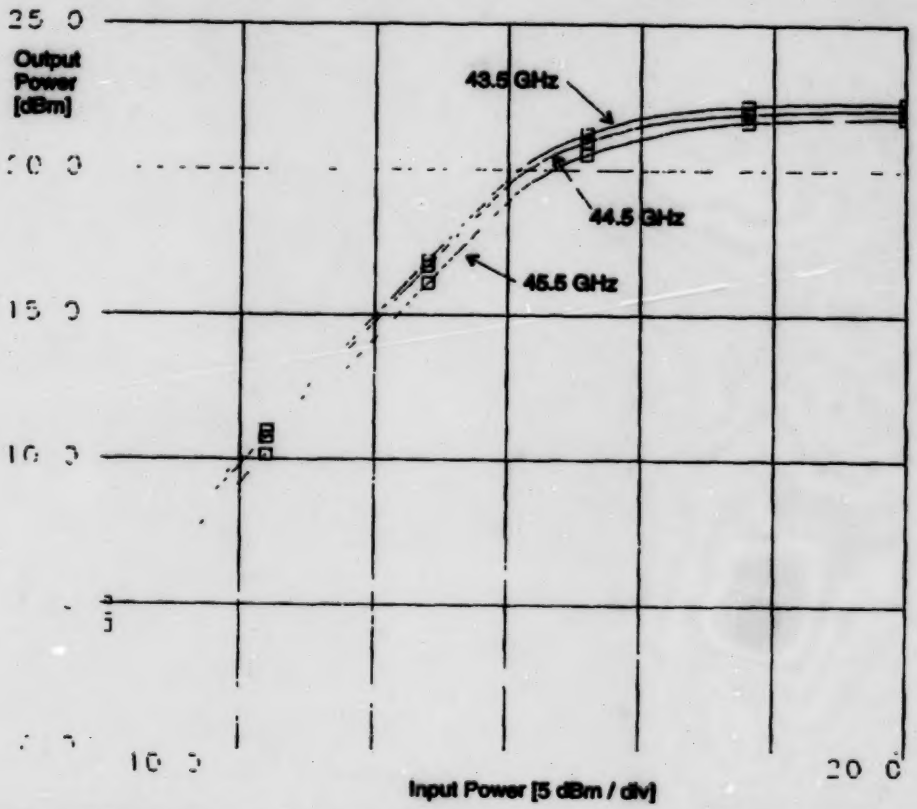

Figure 31: Output power as a function of input power over the desired bandwidth

Table 1: Large signal performance of the two stage amplifier as a function of frequency

Frequency [GHz]	Input Power [dBm]	Output Power [dBm]	Power Gain
42.5	8.00	20.61	12.61
43.5	8.00	20.60	12.60
44.5	8.00	20.35	12.35
45.5	8.00	20.01	12.01
46.5	8.00	19.56	11.56

H. Electromagnetic Simulations

Critical sections of the amplifier were analyzed using the SONNET™ electromagnetic simulator. Specifically, the following sections were examined:

- the entire input matching network
- the entire output matching network
- the entire interstage matching network
- all dc blocking capacitors
- the quarter wavelength chokes
- the resistor-capacitor stabilization network

All coupling of transmission lines within these sections was accounted for. However, coupling between these sections was not considered due to time and memory constraints. The via holes were not analyzed for the same reasons.

The substrate for the microstrip lines was GaAs only. The substrate for the capacitors consisted of GaAs, a layer of Si_3N_4, and a layer of air for the air bridges. The minimum cell size used was 5 μm^2 in all cases.

The matching networks were optimized using SONNET™. The resulting amplifier small signal performance is shown in Figures 32 and 33. The EM optimized large signal performance is given in Figure 34 and Table 2.

The critical sections were also analyzed from 1 GHz to 60 GHz to check stability, and these results are presented in Figure 35.

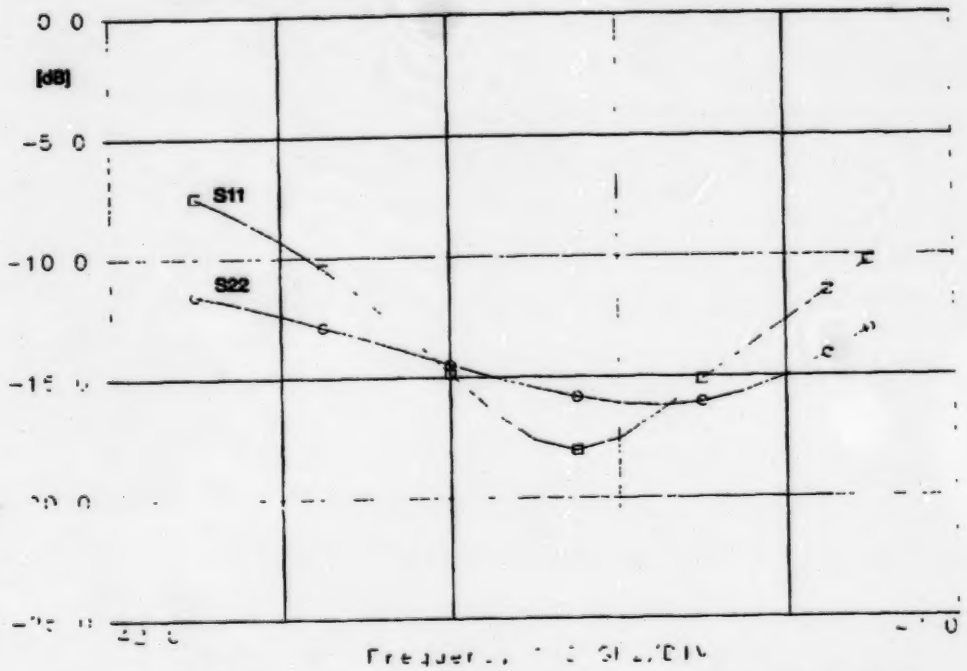

Figure 32: EM simulated amplifier performance after optimization

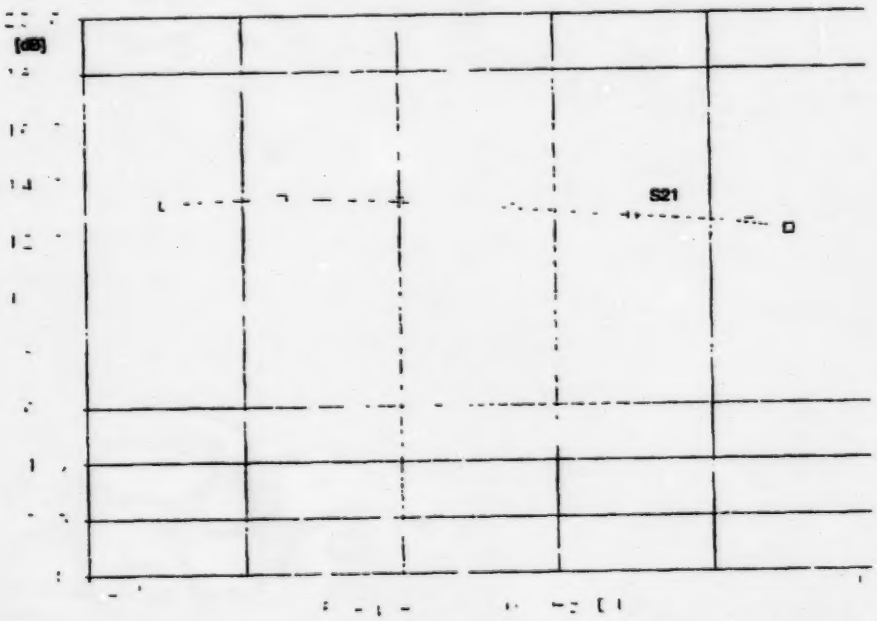

Figure 33: EM simulated amplifier performance after optimization

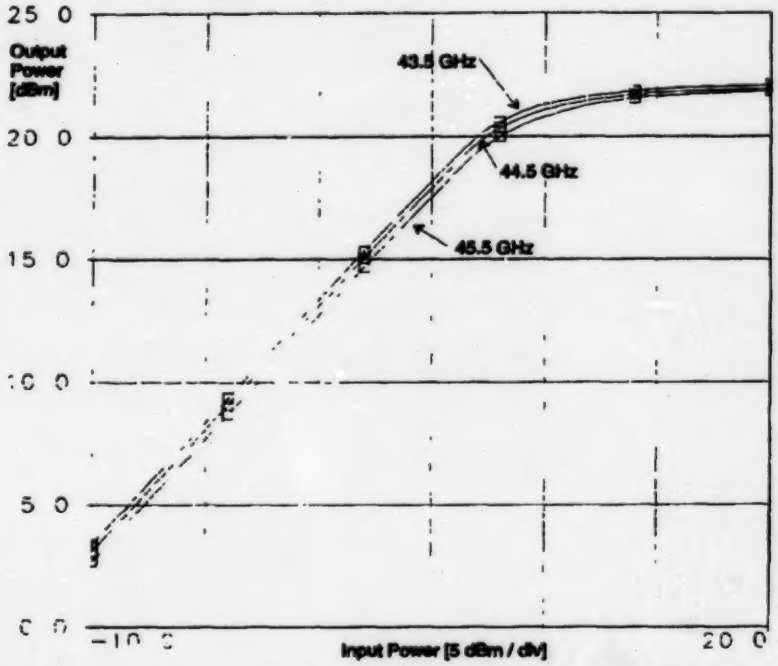

Figure 34: Amplifier large signal performance after EM optimization

Table 2: Large signal performance of the two stage amplifier as a function of frequency after EM optimization

Frequency [GHz]	Input Power [dBm]	Output Power [dBm]	Power Gain
42.5	12.00	20.81	8.81
43.5	12.00	20.45	8.45
44.5	12.00	20.04	8.04
45.5	12.00	19.68	7.68
46.5	12.00	19.37	7.37

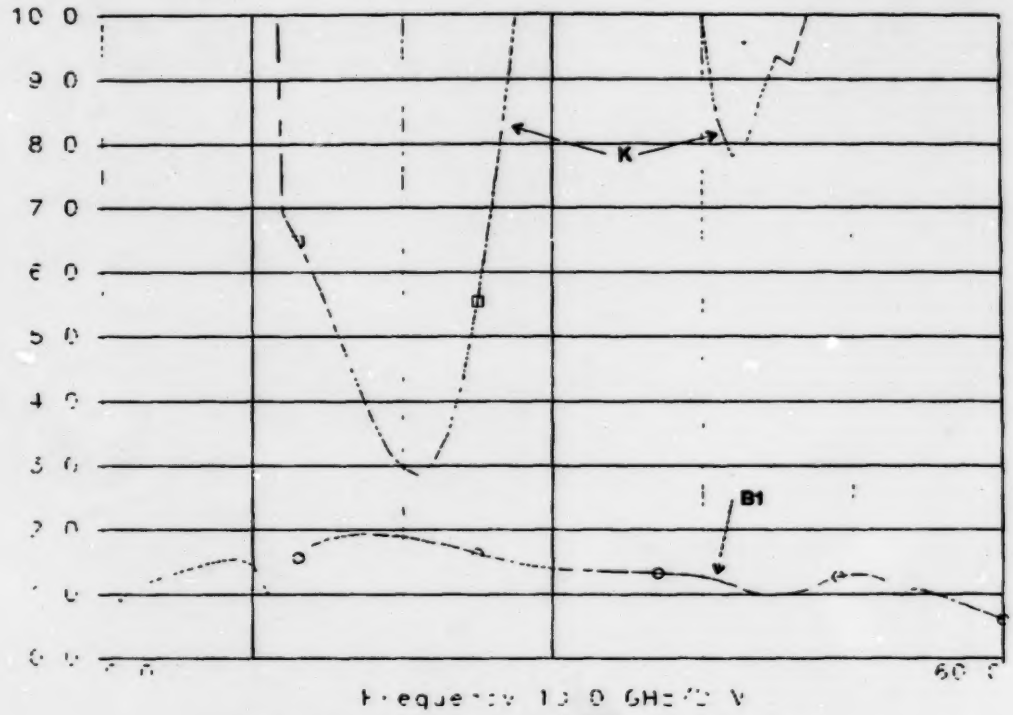

Figure 35: Amplifier stability from EM analysis

I. Amplifier Layout

Using the results from the electromagnetic optimization a final layout for the two stage amplifier was achieved and is shown in Figure 36.

J. Amplifier With Interconnects

The amplifier was altered slightly to account for bond wire interconnects. The stub lengths were optimized to reduce the performance degradation due to the bond wire inductances. Figures 37 and 38 show the simulated small signal performance with bond inductances of 0.15 nH. Figure 39 gives the large signal amplifier performance with interconnects and the simulated stability is shown in Figure 40. All results are from electromagnetic simulations. A final layout for the amplifier with interconnects is provided in Figure 41.

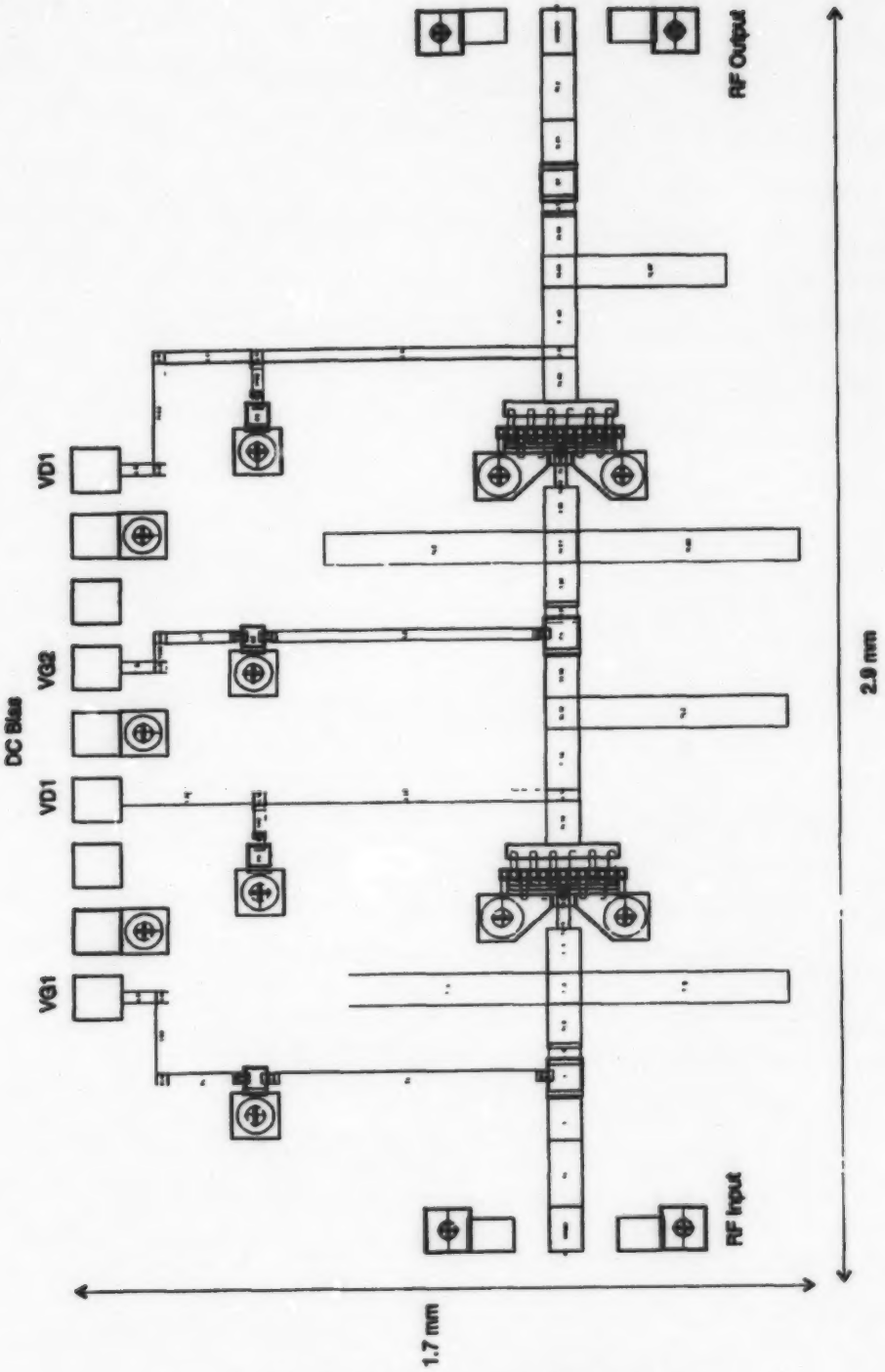

Figure 36: Final two stage amplifier layout

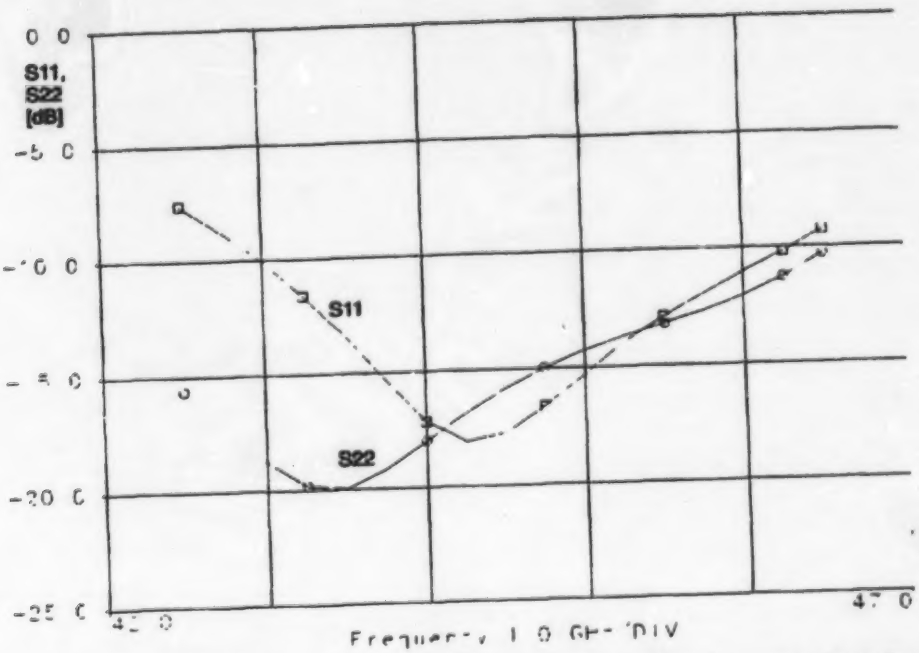

Figure 37: Small signal performance of the amplifier with interconnects (after EM optimization)

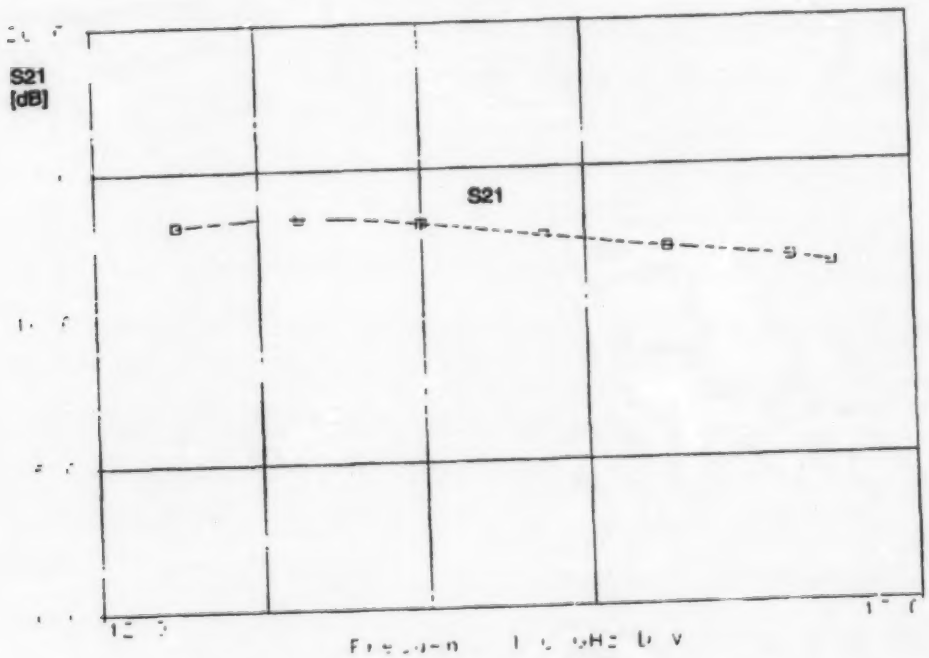

Figure 38: Small signal performance of the amplifier with interconnects (after EM optimization)

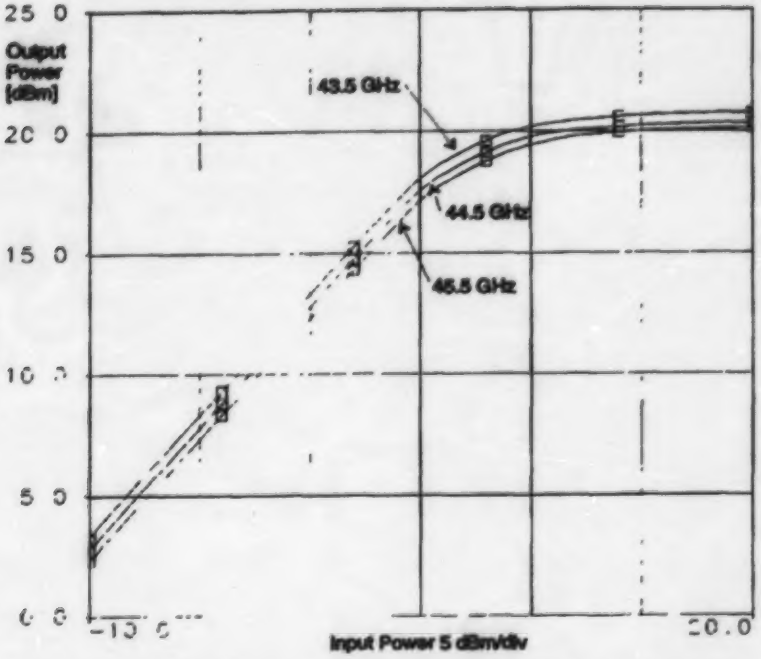

Figure 39: Large signal performance of the amplifier with interconnects (after EM optimization)

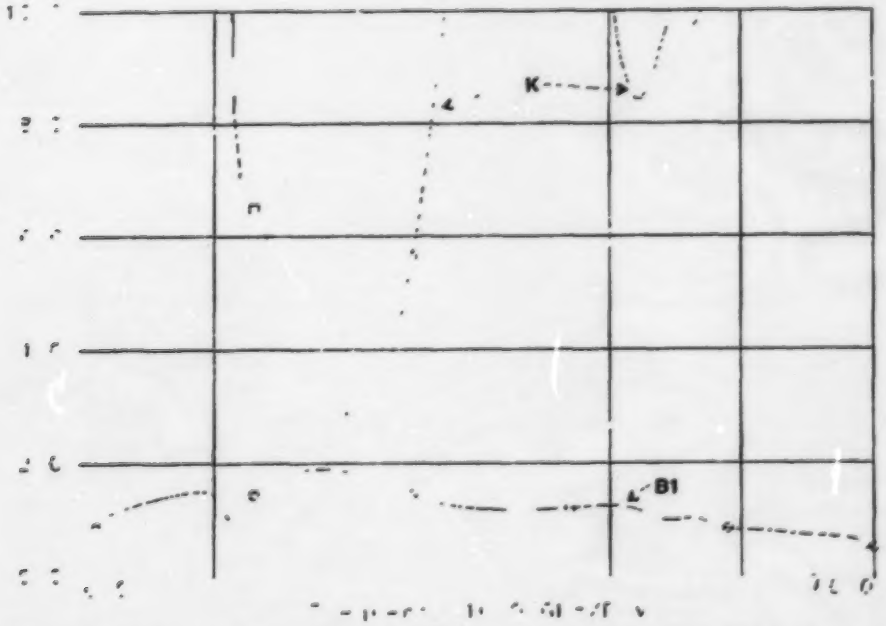

Figure 40: Stability of the amplifier with interconnects (after EM optimization)

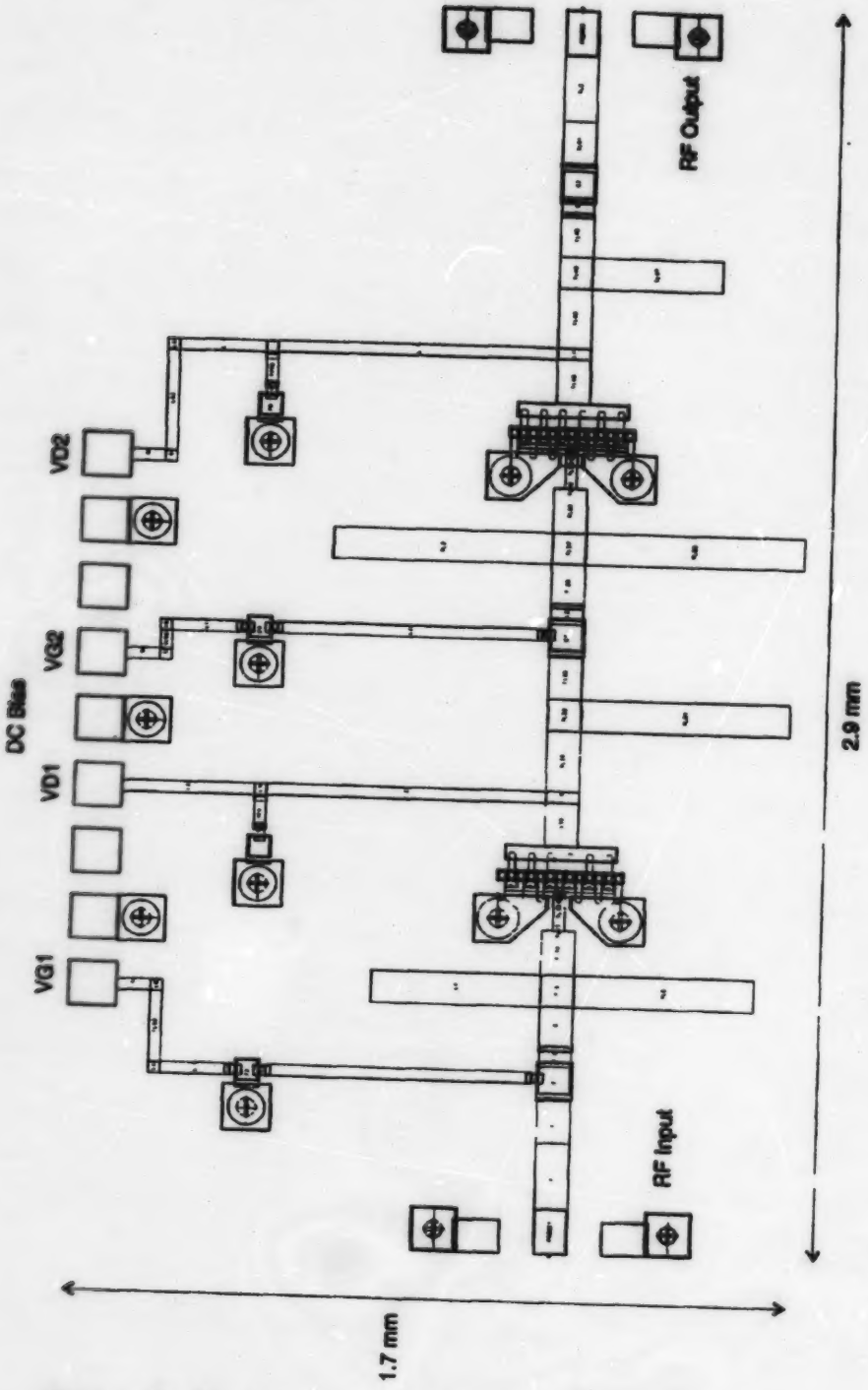

Figure 41: Final layout of the amplifier with interconnects

Dual Amplifier Chain Performance

The performance of two amplifiers connected in series was briefly investigated. The amplifiers modified for interconnects were used and the resulting EM simulated small signal performance is shown in Figures 42 and 43.

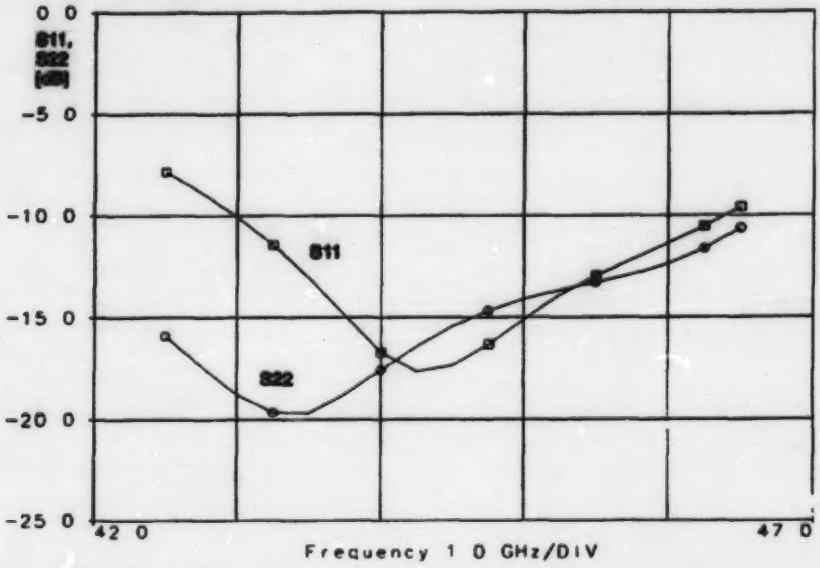

Figure 42: Small signal return loss performance of two amplifier chain with interconnects

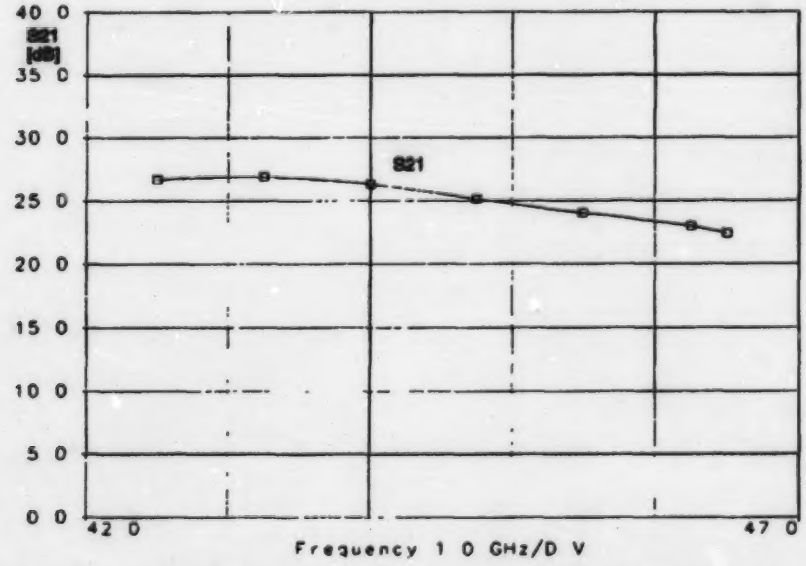

Figure 43: Small signal gain performance of two amplifier chain with interconnects

III. Fabricated Circuits

The two versions of the power amplifier, one with matching networks designed for wafer probing and one with matching networks designed for measurement in a jig, were fabricated at Northrop Grumman. Photographs of the circuits are included as Figures 44 and 45, respectively.

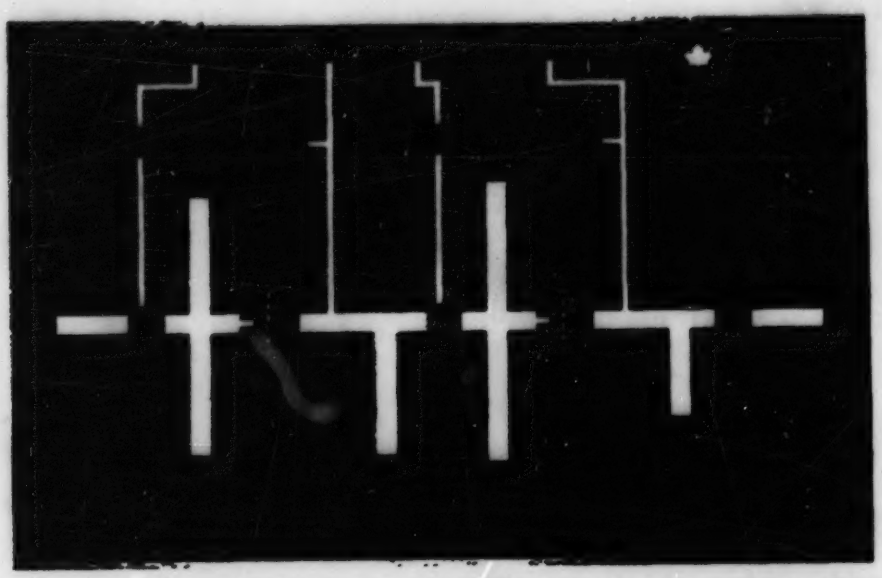

Figure 44: Photograph of power amplifier intended for wafer probing

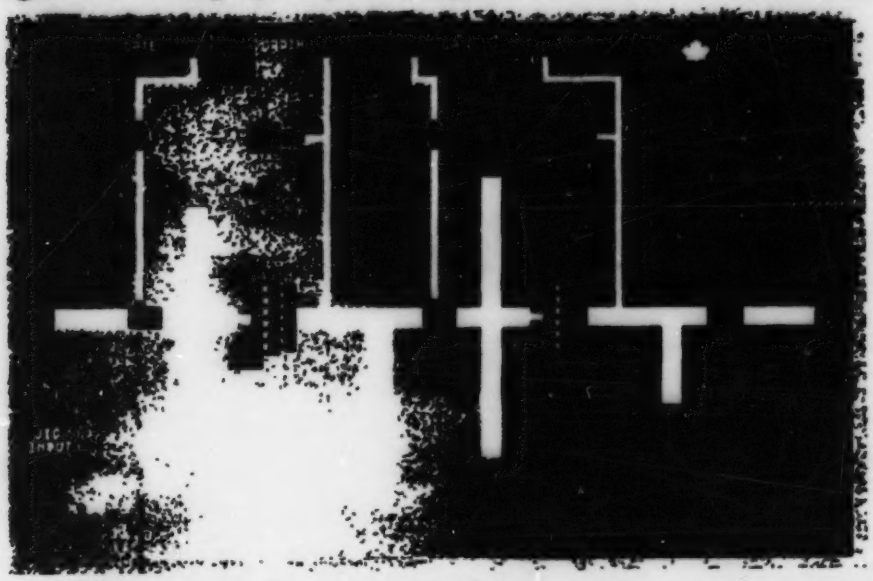

Figure 45: Photograph of power amplifier intended for measurement in a jig

IV. Measurements

The amplifier was fabricated by Northrop Grumman using their 0.25 micron PHEMT process. There was an extreme delay of over one year in the processing because of the failure of the company's electron beam writing machine. This machine is used to define the PHEMT gate structures – the most critical structure of the transistor since it determines its high frequency response. Repair to this machine took several months and, unfortunately, Northrop Grumman did not have a second source available for this step. A total of 4 wafers were eventually delivered by the company.

A. Wafer 1

The first wafers to be fabricated after repair of the e-beam machine did not pass process control monitor (PCM) specifications but because of the extended delays incurred, Northrop Grumman was persuaded to send us a wafer for exploration purposes. Appendix 1 shows details of the measured results.

The wafer was initially sampled in 5 locations to determine the appropriate bias conditions. The results show measurements for chips R3C5, R2C2, R5C2, R6C7 and R3C2, all chips showing similar performance with gains between 7.5 and 8.5 dB at 44.5 GHz and input and output return losses around –10 dB. Comparing the measured results to the design predictions, the measured input and output return losses are about 5 to 8 dB worse than those predicted in Figure 32 and are lower in frequency by a few hundred MHz. The measured gain response shows a significant difference from the predicted value of about 13 dB (Figure 33), never reaching more than 10 dB anywhere in the frequency response.

It was observed that the amplifier response was not very sensitive to drain bias and so all the operational chips across the wafer were automatically probed at a bias of Vds = 3v, Vgs = - 0.5v, similar to the original design biases. The results are shown in Appendix 2 for both the amplifier designed to be measured on-wafer (plot labeled "wfr0") and the chip designed to be measured in a jig (entitled "amplifier with interconnects" in Section II, J and shown on the measurement plot labeled "jig0"). These results show gain curves for several chips, the gain differing between chips – from about 1 dB to 8 dB at 43.2 GHz for the "wfr0" chips and from about 2.5 dB to 8 dB for the "jig0" chips. This illustrates some of the results of the process variations across the wafer which are to be expected because the wafer did not meet the delivery requirements.

B. Wafers 3, 4 & 5

Two wafers which met PCM specifications were delivered a few months later along with a third wafer that did not quite pass. This situation again suggested that the process was still not fully stabilised.

Note that the wafer identification numbers relate to a wafer's location in the process batch and we have kept to Northrop Grumman's numbering system. Thus, the absence of "wafer 2" has no meaning in terms of this report.

Each of the wafers was probed automatically and the results for each are shown in Appendices 3, 4 and 5.

In general, the frequency responses of the chips were similar to that of Wafer 1. However, individual probing showed that it was not possible to achieve the same amplifier gains as that observed with Wafer 1, even though the bias conditions were optimised for each chip. Some chips, for example, gave 0 dB above 43.5 GHz. If the bias was adjusted to achieve the absolute maximum gain at the high end of the curve, the response became very peaked around 45 GHz. It can also be seen that the input reflection coefficient (S11) plots achieve their minimum at slightly different frequencies – from around 39.5 GHz to around 43.6 GHz. Since the differences related to differences in wafers, it again points to process variations.

V. Conclusions

The amplifiers showed gains which were dramatically lower than the theoretical predictions but the overall shapes of the gain and the return loss curves are similar to those expected, suggesting that the designs were valid. Larger than usual variations in gain were also observed across a wafer (up to 5 dB). This variation is often indicative of processing problems and since Northrop Grumman had great difficulty with their fabrication line, it is the most likely cause. It is useful to note that the chips showing the largest gains around 40.5 – 45.0 GHz were, in fact, those on the wafers which did not meet PCM specifications!

Appendix 6 shows the PCM data for wafers 3,4 and 5 and it can be seen that the data which relates specifically to the PHEMT rather than the passive components (i.e. maximum available gain, drain-gate breakdown voltage and source-gate breakdown voltage) indicates low yields. Measurements of individual 500 μm transistors indicated a significant variation of output impedance and this could be the main reason for the poor performance. One other possible cause is the fact that Northrop Grumman advised us to use a 25 μm unit gate width for the transistors because of the high frequency application. Since the usual unit gate width is 50 μm, this change will affect the model of the device and will also affect the processing characteristics of the transistor as the gate etching rate varies with unit gate width. Further characterization and modeling of the transistor is required to confirm these statements followed by a second design and fabrication.

Appendix A: Performance of Individual Chips on Wafer 1 Versus Frequency

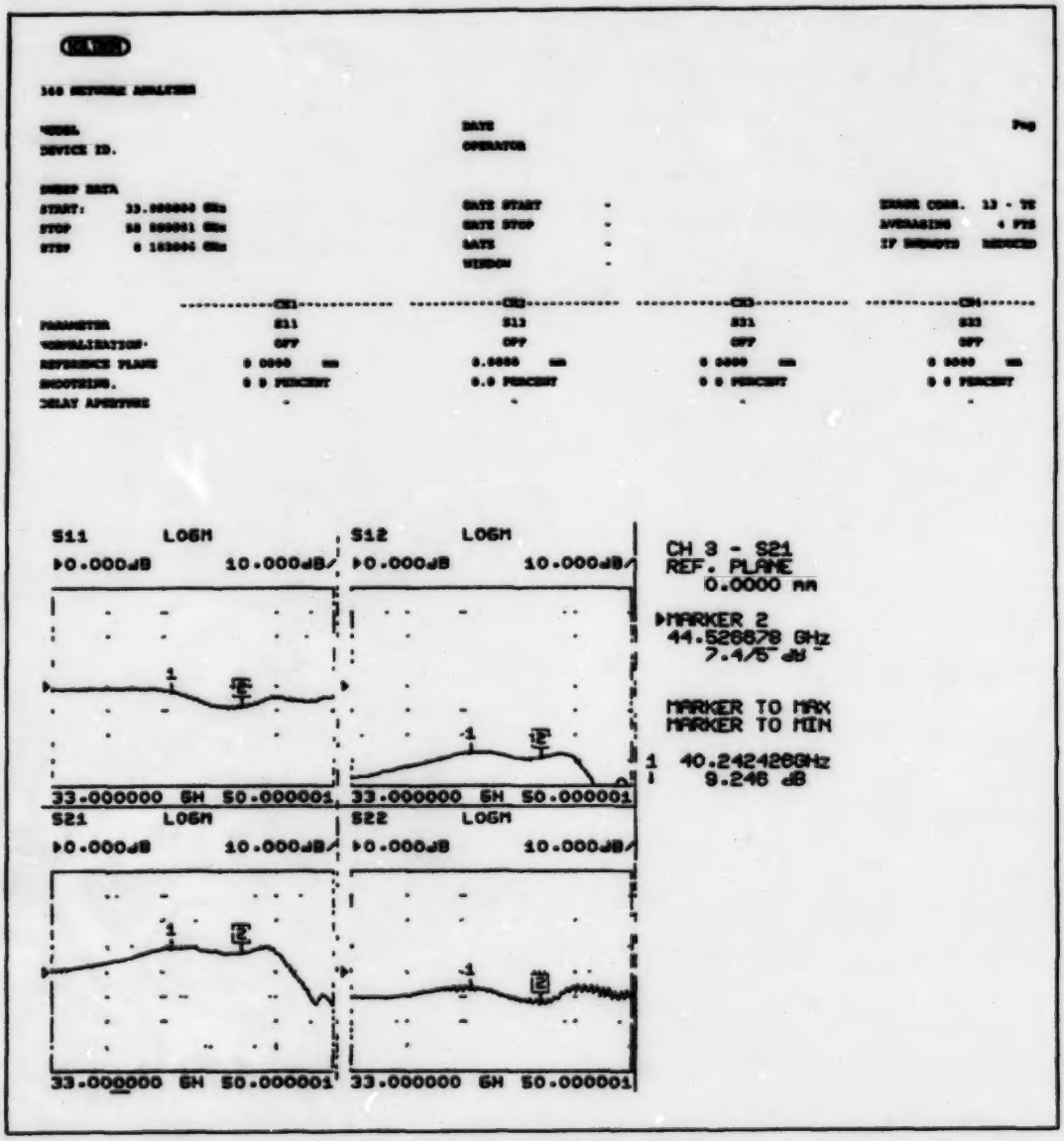

Figure 46: SSPA S-parameters vs frequency [Jig = R3C5, V_D = 2.0 volts, V_G = -0.5 volt, I_{DS} = 221 mA]

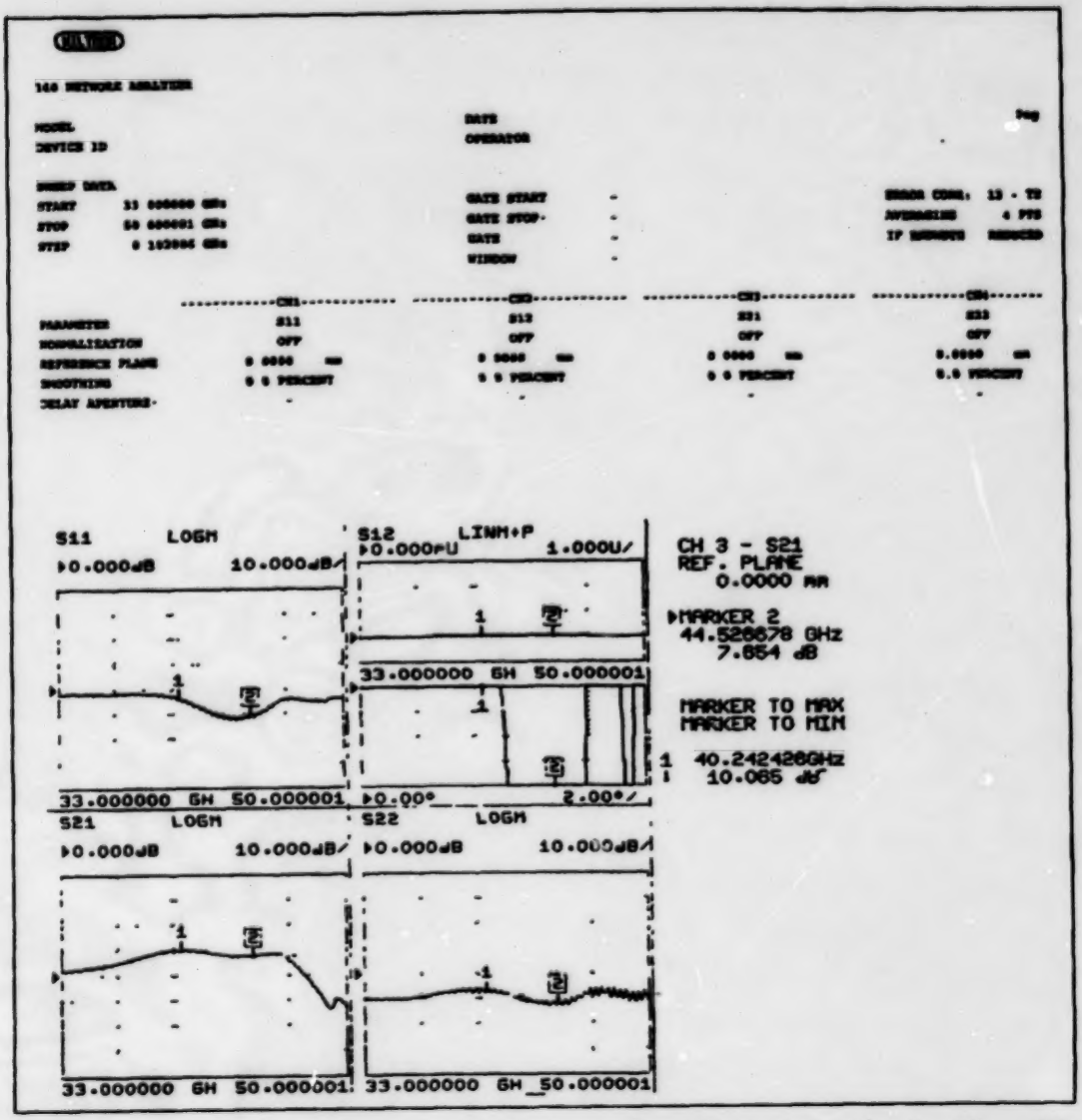

Figure 47: SSPA S-parameters vs frequency [Jig = R2C2, V_D = 2.0 volts, V_G = -0.5 volt, I_{DS} = 150 mA]

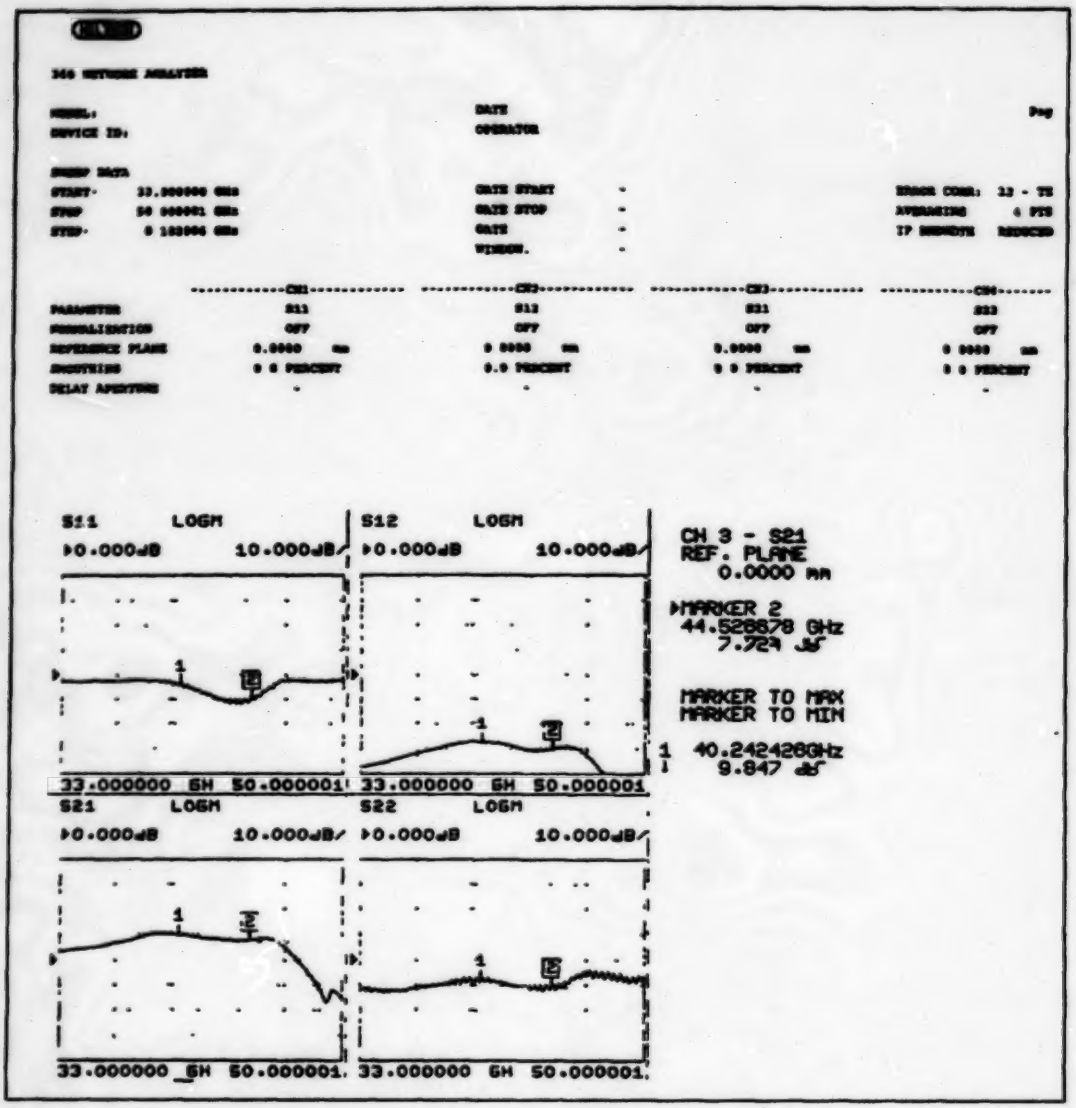

Figure 48: SSPA S-parameters vs frequency [Jig : R5C2. V_D = 1.2 volt, V_G = -0.5 volt, I_{DS} = 131 mA]

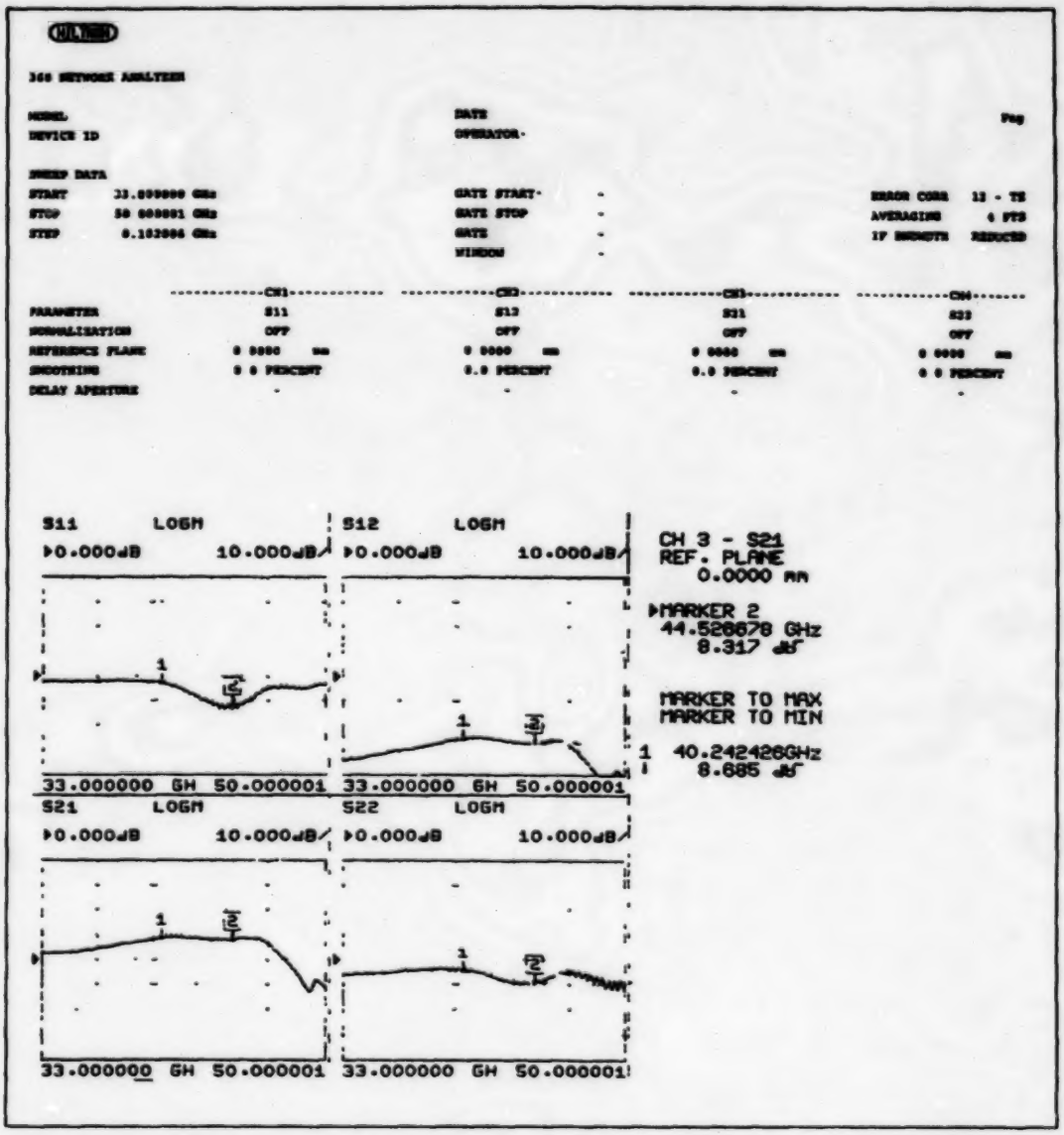

Figure 49: SSPA S-parameters vs frequency [Jig = R6C7, V_D = 1.4 volts, V_G = -0.6 volt, I_{DS} = 70 mA]

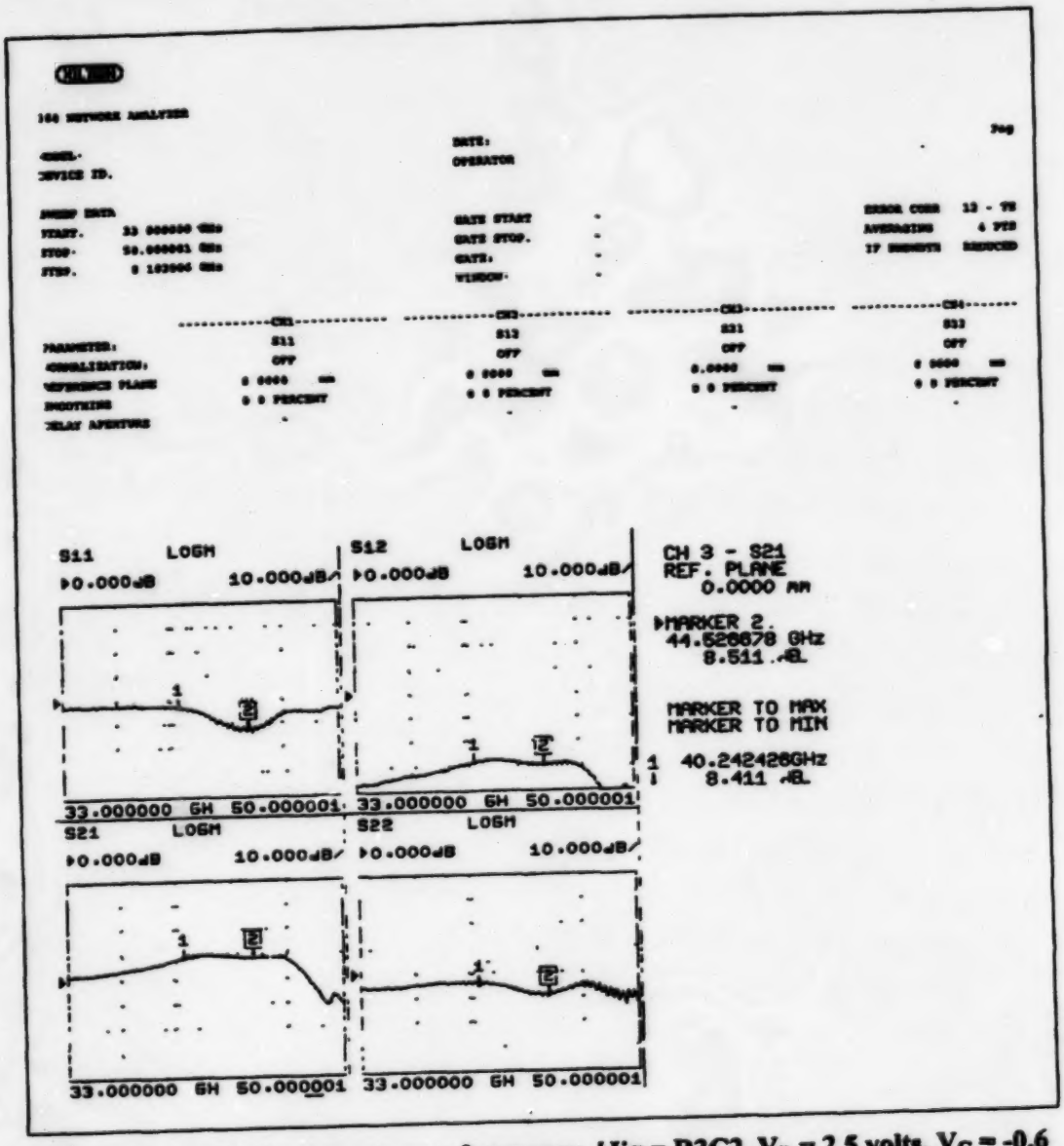

Figure 50: SSPA S-parameters vs frequency [Jig = R3C2, V_D = 2.5 volts, V_G = -0.6 volt, I_{DS} = 90 mA]

Appendix B: Performance of Multiple Chips (wfr0 and jig0) on Wafer 1 Versus Frequency

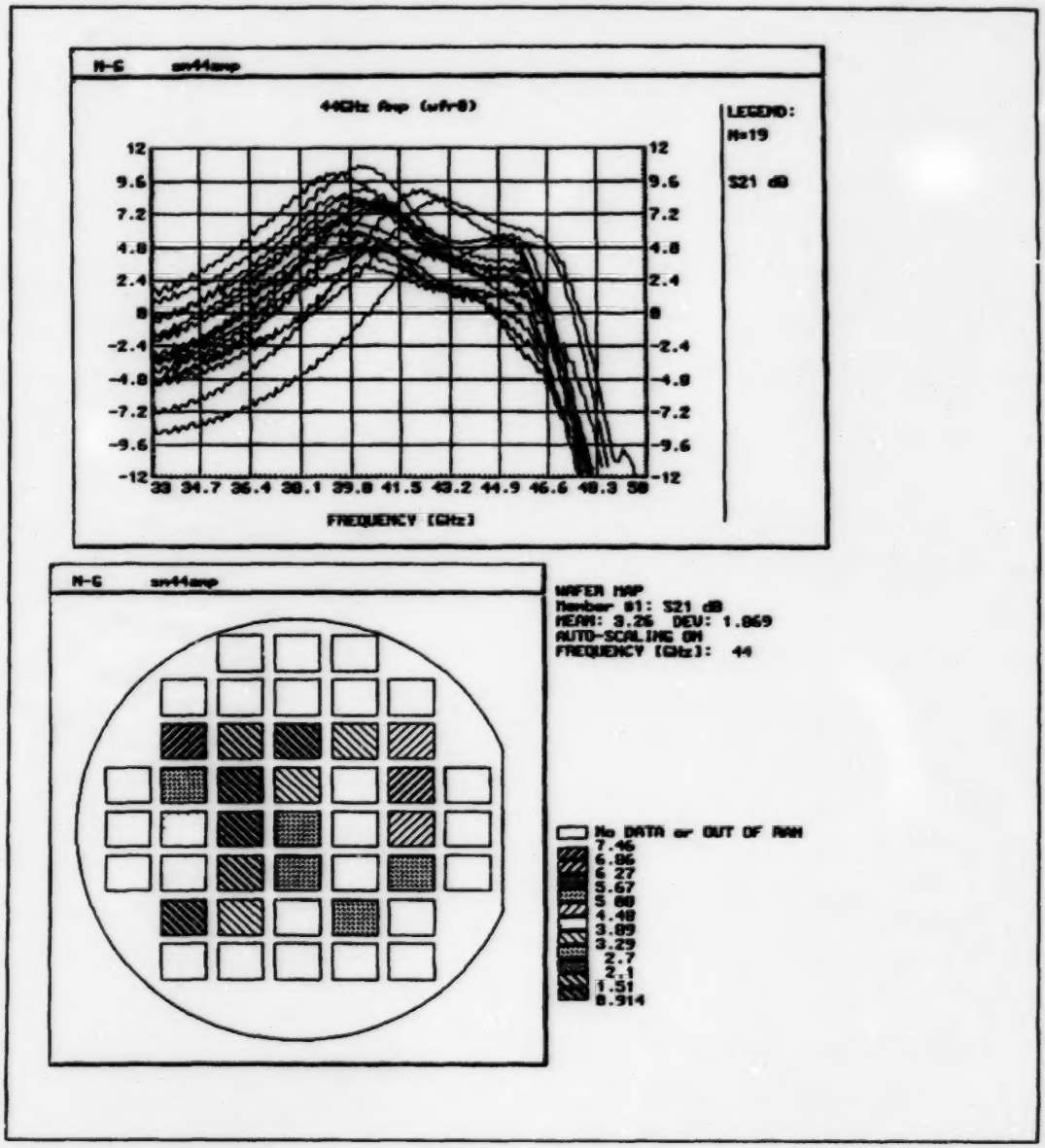

Figure 51: SSPA gain for Wafer 1 - wfr0. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom)

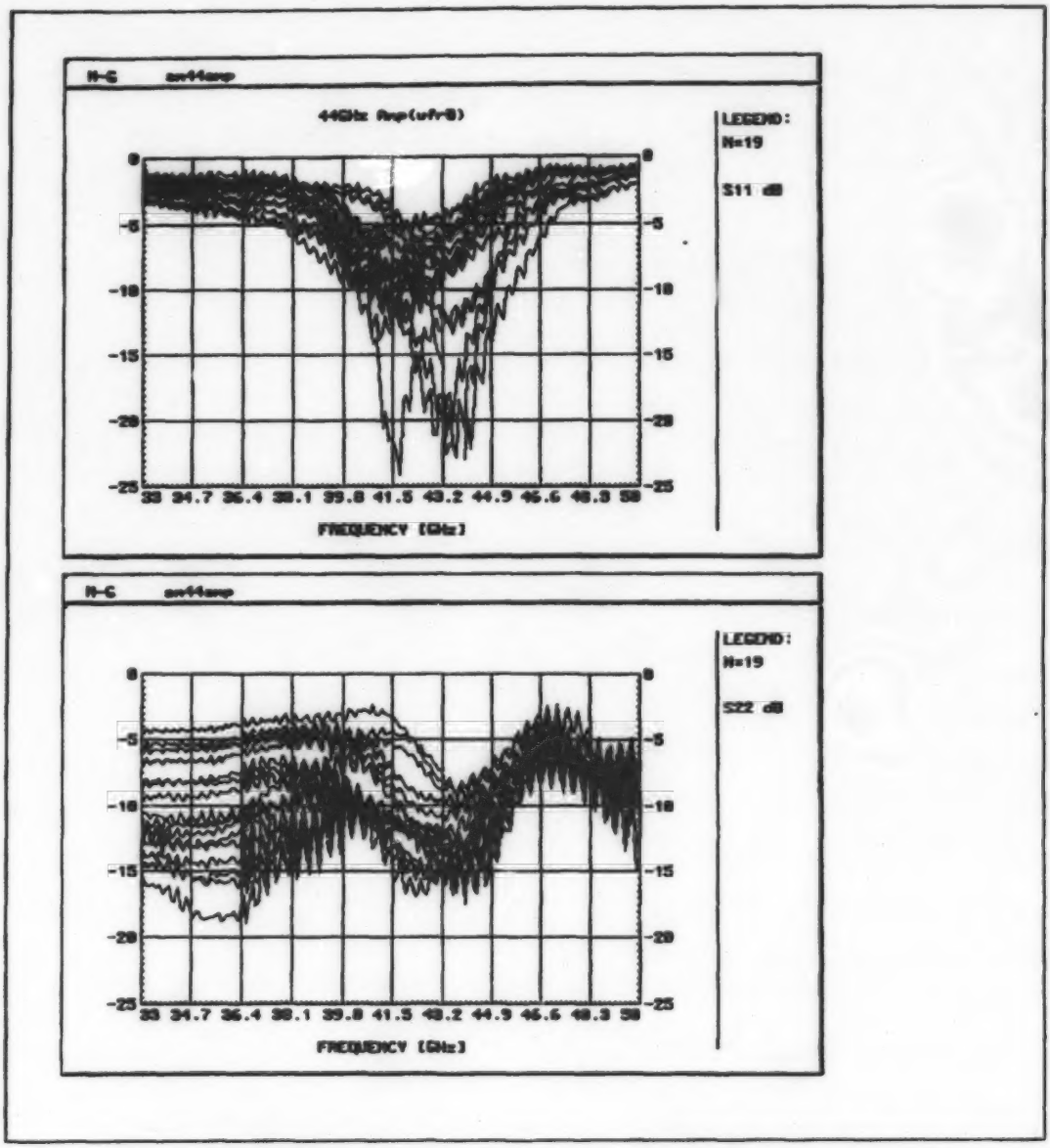

Figure 52: SSPA input and output return losses for Wafer 1 - wfr0

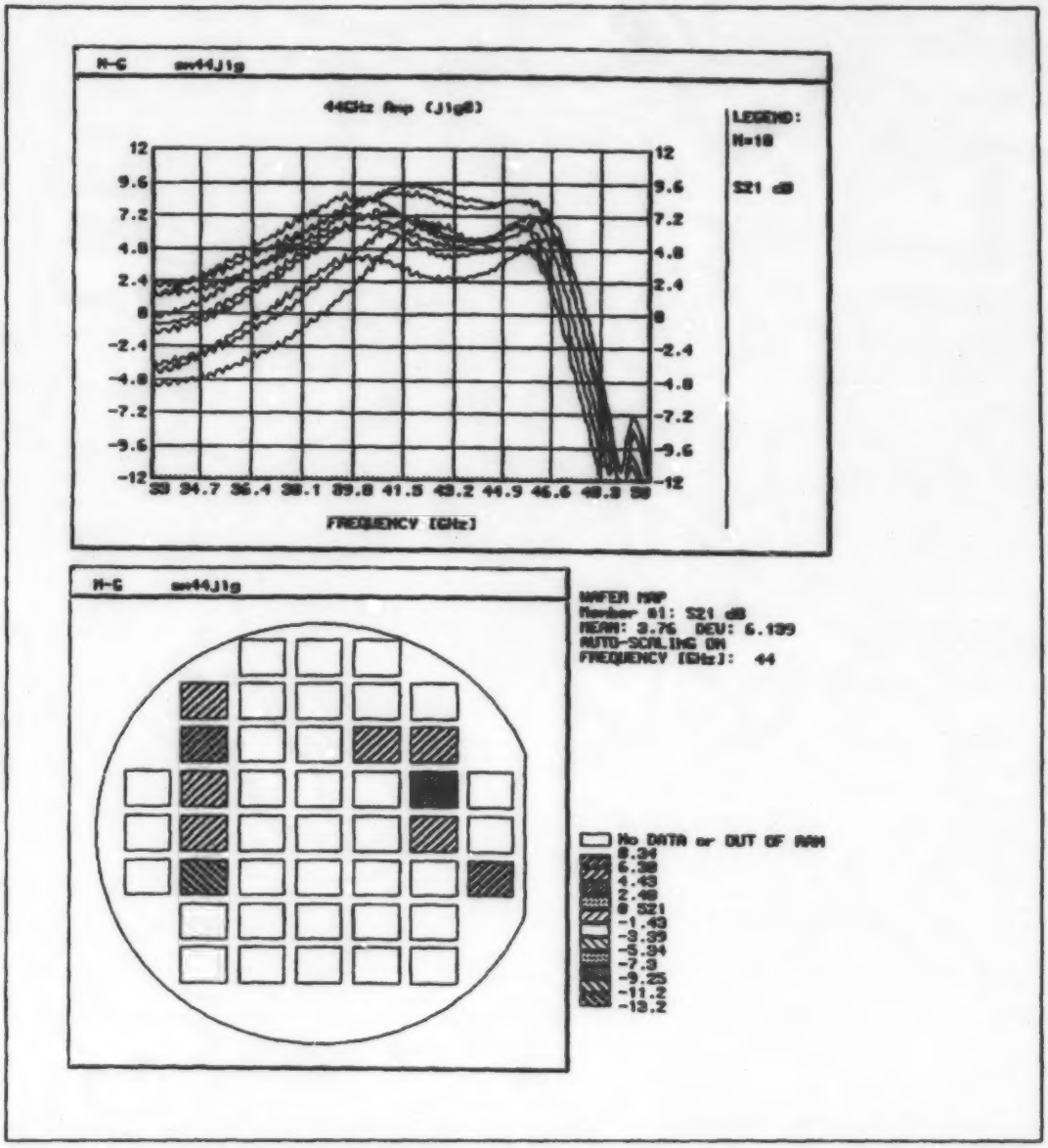

Figure 53: SSPA gain for Wafer 1 - jig0. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom)

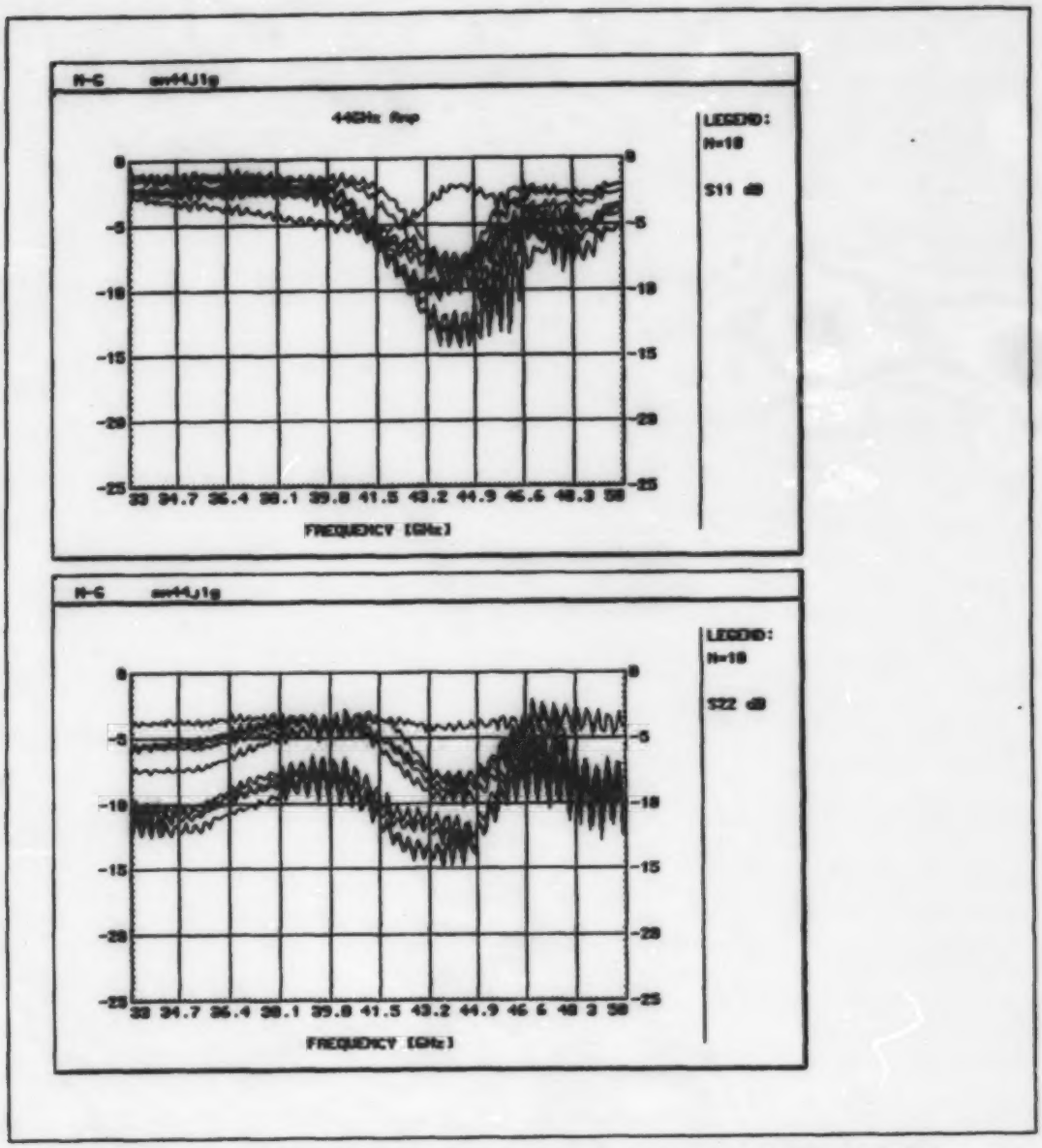

Figure 54: SSPA input and output return losses for Wafer 1 - jig0

Appendix C: Performance of Multiple Chips on Wafer 3 Versus Frequency

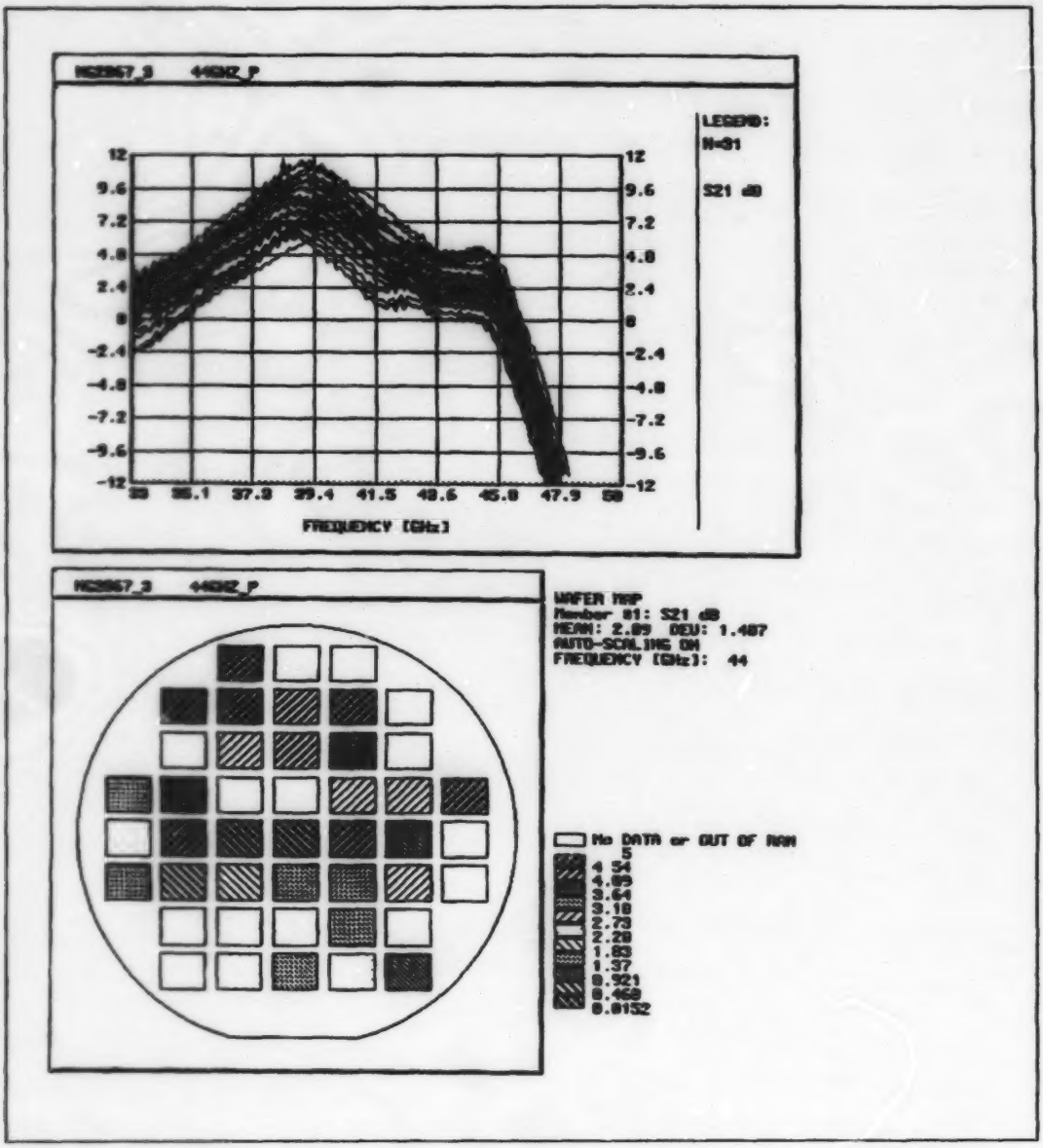

Figure 55: SSPA gain for Wafer 3. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom)

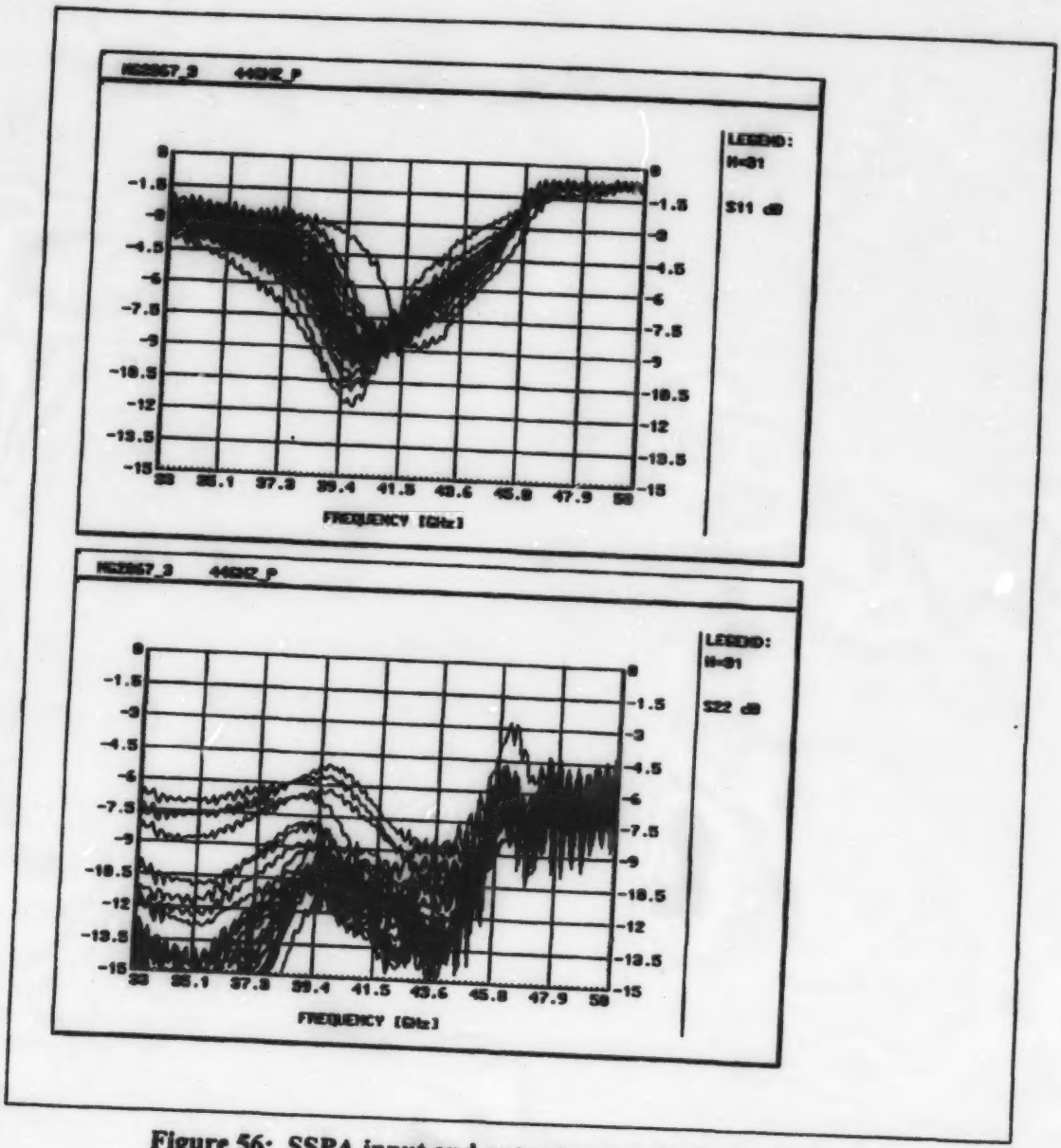

Figure 56: SSPA input and output return losses for Wafer 3

Appendix D: Performance of Multiple Chips on Wafer 4 Versus Frequency

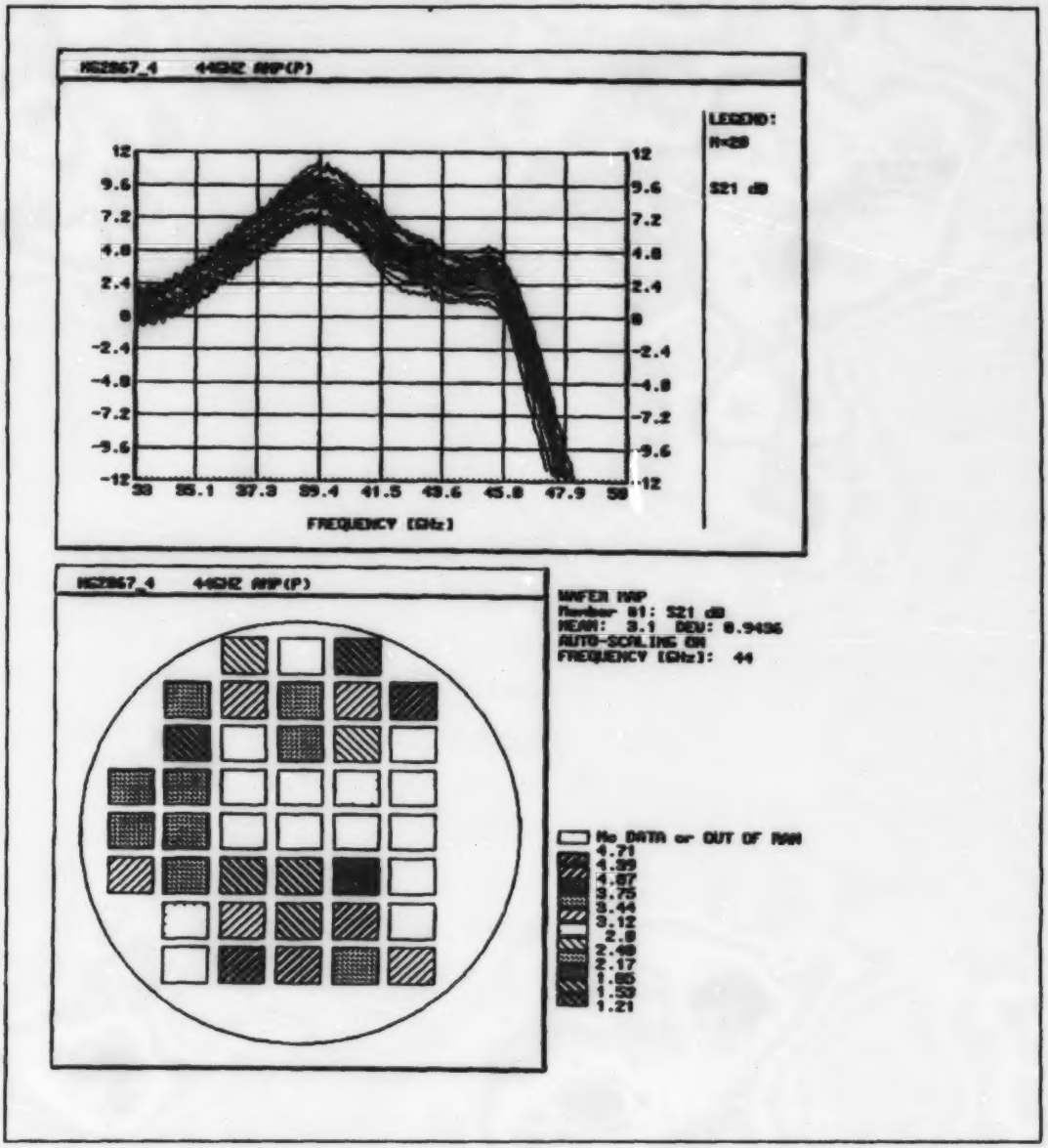

Figure 57: SSPA gain for Wafer 4. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom)

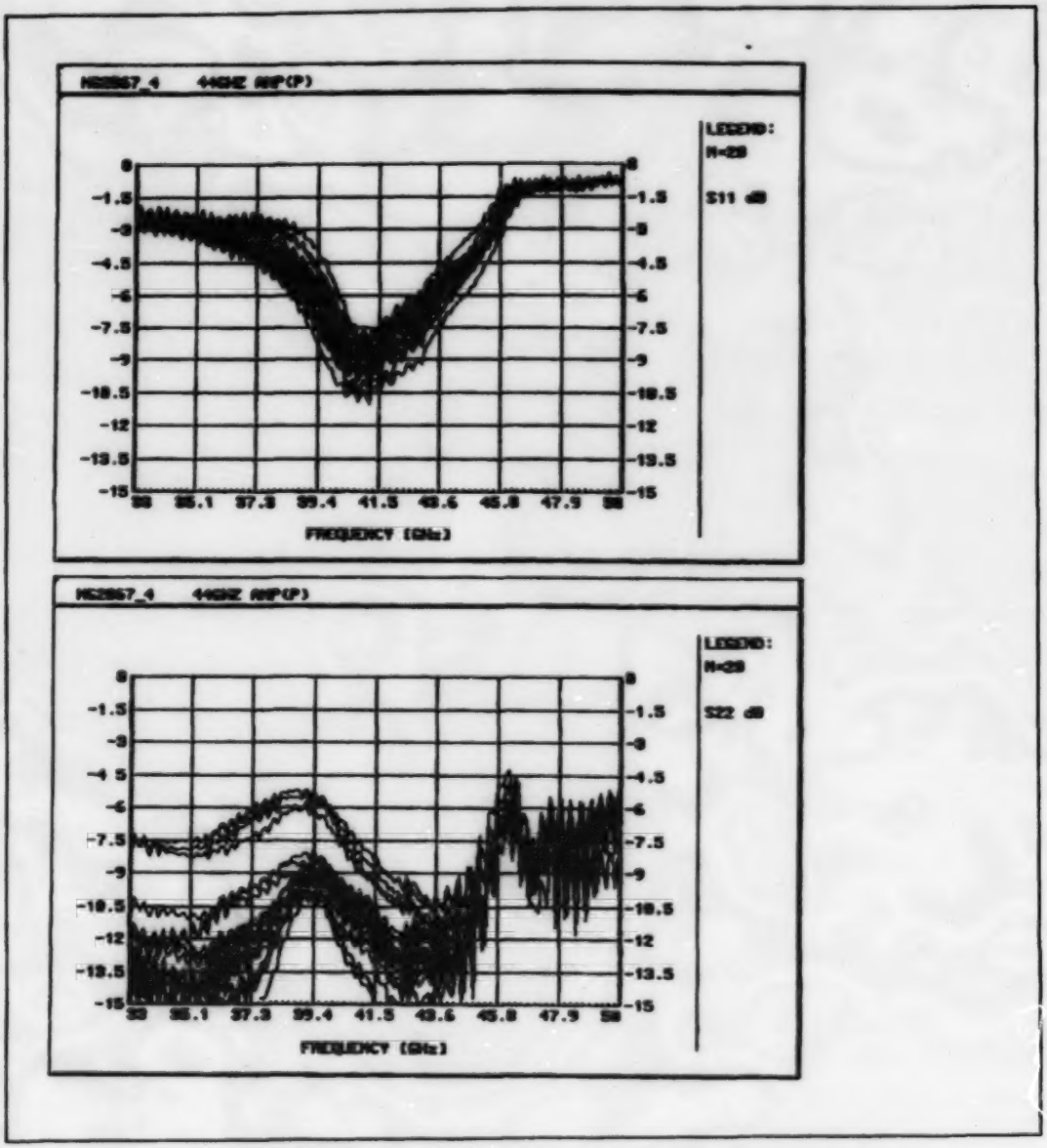

Figure 58: SSPA input and output return losses for Wafer 4

Appendix E: Performance of Multiple Chips on Wafer 5 Versus Frequency

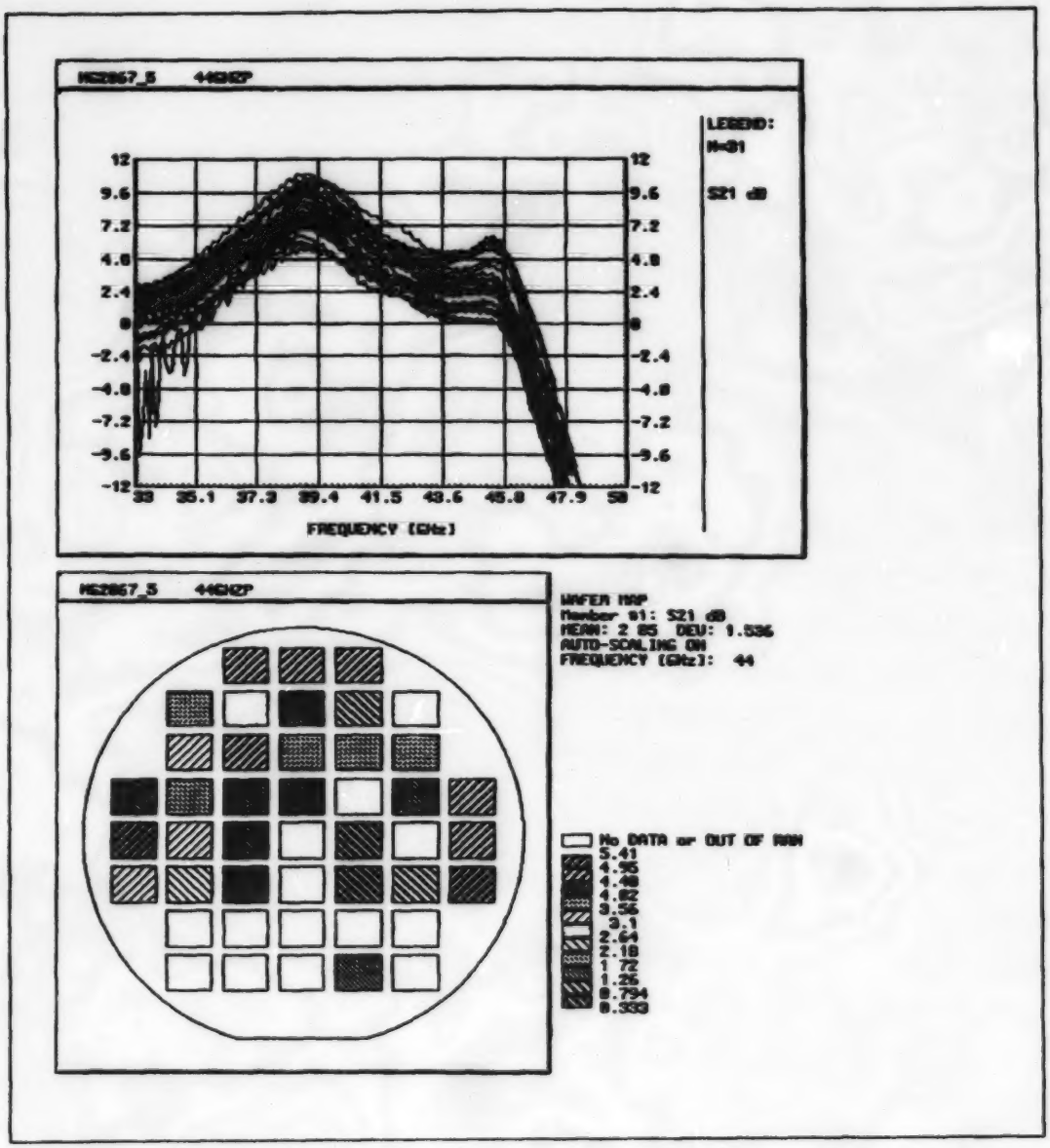

Figure 59: SSPA gain for Wafer 5. Gain vs frequency (top) and Wafer Map showing the gain distribution across the wafer (bottom)

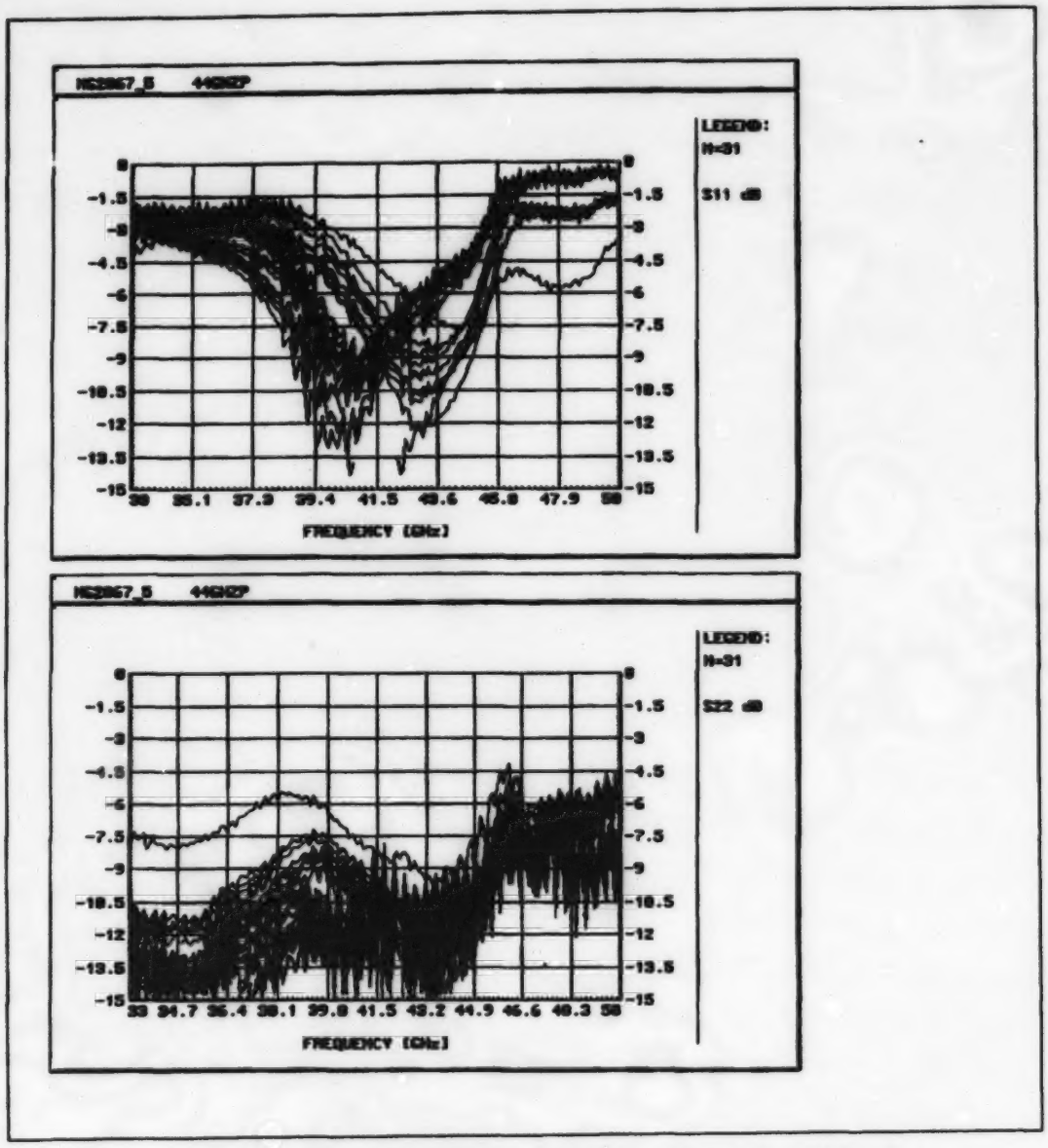

Figure 60: SSPA input and output return losses for Wafer 5

Appendix F: PCM Data for Wafers 3, 4 and 5

Table I (cont) - PHEMT Parameters

Parameter	Acceptable Range*	Test Method	PCM Yield
Active layer sheet resistance (ohms/sq) Used for Type 1 resistor	160 ± 15%	van der Pauw ph_5ab_mask_dc_pcm/rsnpnm	>50%
Metal film sheet resistance (ohms/sq) Used for Type 4 resistor	10 ± 3	2.5 square resistor ph_5ab_mask_dc_pcm/t25tfr	>50%
7.5 pF MIM Capacitor	7.5 ± 10%	1 MHz LCR meter ph_6cp_mask_dc_pcm/iso7_5pf	>50%
Maximum available gain at 12 GHz (dB)**	15 min	S-parameters Vds=5V; Ids=50%Idss ph_9rfdm_mask_pe_500um_10x50/mag50	>25%
Drain Gate Breakdown Voltage (V)	>10	Is=0; Id=0.1mA/mm ph_9rfdm_mask_pe_500um_10x50/bvdg0	>25%
Source Gate Breakdown Voltage (V)	>7	Id=0; Is=0.1mA/mm ph_9rfdm_mask_pe_500um_10x50/bvsgo	>25%
Intact reticles	70% min	Visual	N/A

* The mean value of a set of measurements taken over the wafer of each parameter shall fall within the range specified.

** These measurements are made on a PHEMT cell which has ten .25um x 50um gate fingers in a common-source configuration. This cell is capable of providing 200mW at 30 GHz with greater than 30% power added efficiency.

Figure 61: PHEMT parameters from manufacturer's documentation

PCM Data

Lot 2067 Mask 6852 GD 56568

Communication Research Centre CRC PO# U6800-6-3946

Active Layer Sheet Resistance (160 ohm/sq)

lot_number	wafer_num	AvgOfrsnnnm	CountOfrsnnnm	PCM Yield Sheet Resistance
2067	3	155.14	44	100.00
2067	4	155.58	44	100.00
2067	5	157.61	44	100.00

25 ohm Metal Film Resistor

lot_number	wafer_num	AvgOfr25tfr	CountOfr25tfr	PCM Yield Metal Film Resistor
2067	3	25.75	44	100.00
2067	4	26.37	44	100.00
2067	5	26.49	44	100.00

7.5 pF Capacitor

lot_number	wafer_num	AvgOfcap7_5pf	CountOfcap7_5pf	PCM Yield 7p5 Cap
2067	3	7.09	28	93.33
2067	4	7.09	29	96.67
2067	5	7.10	30	100.00

Maximum Available Gain (15 dB min)

lot_number	wafer_num	AvgOfmag50	CountOfmag50	PCM Yield MAG
2067	3	17.04	26	57.78
2067	4	TBD		
2067	5	16.81	33	73.33

Drain-gate Breakdown Voltage (10 V min)

lot_number	wafer_num	AvgOfbvdg0	CountOfbvdg0	PCM Yield bvdg0
2067	3	11.87	26	57.78
2067	4	TBD		
2067	5	11.79	22	48.89

Source-gate Breakdown Voltage (7 V min)

lot_number	wafer_num	AvgOfbvsgo	CountOfbvsgo	PCM Yield bvsgo
2067	3	16.81	22	48.89
2067	4	TBD		
2067	5	15.94	22	48.89

Intact Reticles

Wafer 3 45/45 100%

Wafer 4 30/45 67%

Wafer 5 45/45 100%

Figure 62: PCM data from manufacturer's documentation

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The work described in this report represents the design phase of a gallium arsenide monolithic microwave integrated circuit (GaAs MMIC) power amplifier using pseudomorphic high electron mobility transistors (PHEMTs). The main purpose was to investigate the possible performance of a power amplifier at 44 GHz for future application in a phased array antenna system. The design of a two stage amplifier, covering the frequency range 43.5 - 45.5 GHz, is described along with measured results. The final layout of the complete chip is also presented.

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mmic, sspa, power amplifier

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